ID-Xplore™: A Cognitive Software for Designing First-Time Right Analog IP

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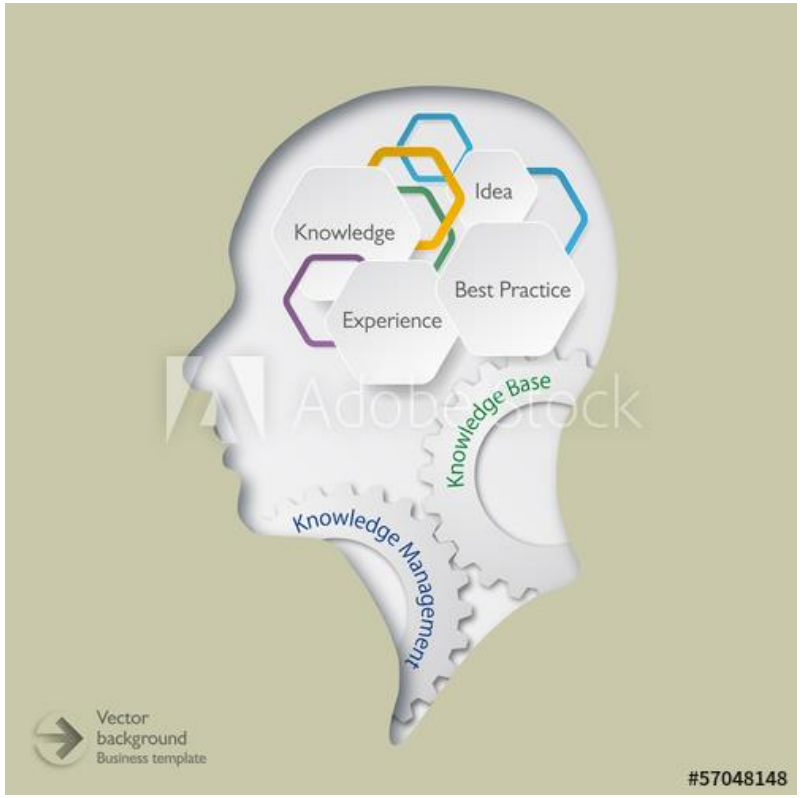
Hierarchy of Intelligence:

- **Machine Learning (ML)** – We are stuck here !
  Lowest level of data mining and classification
- **Artificial Intelligence (AI)**
  Connect algorithms to perform complex tasks
- **Cognitive Intelligence (CI)**
  Reasoning and building different concepts
  in a deterministic and logic manner

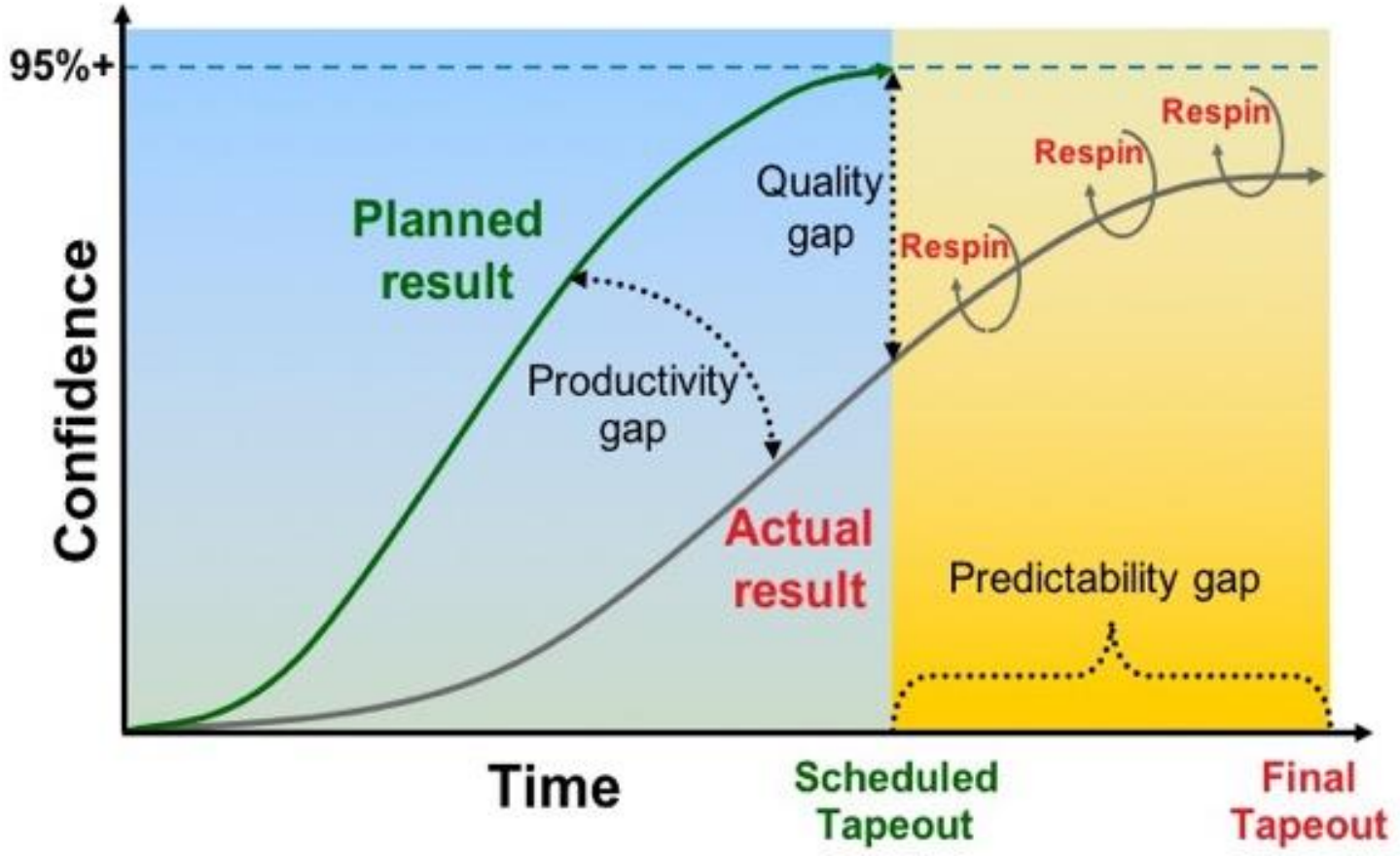
Knowledge can be classified into:

1. **Meta-knowledge:** involves general cultural and philosophical assumptions
2. **Milieu:** is knowledge about the local environment
3. **Tacit knowledge:** is rooted in practice and experience.
4. **Informal knowledge:** is made up of rules of thumb or tricks of the trade
5. **Formal knowledge:** involves theories and proven formulae
6. **Instrumentalities:** embedded in tools and instruments
7. **Contingent knowledge:** is distributed and apparently trivial information specific to a particular environment

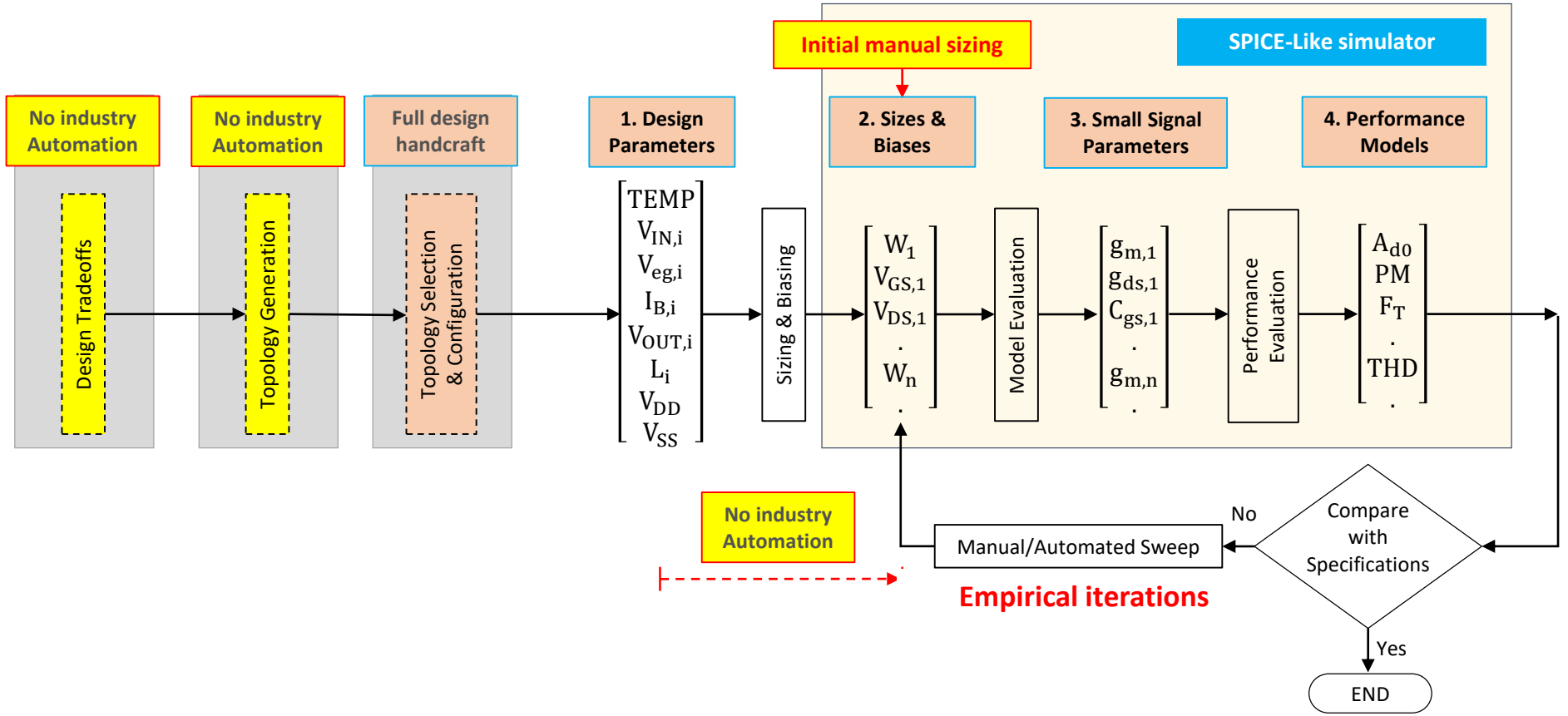
Tacit knowledge



What keeps AMS designers up at night ?



Traditional Analog Design Method



Nonlinear DC Analysis in Spice Simulators

1.From **NR algorithm** : $\boldsymbol{J^k\ \Delta v^k = -f(\ v^k)}$

2.From **LU Decomposition**:

$$\boldsymbol{J \equiv L\ U} \equiv \begin{bmatrix} J_{11}^{(0)} & 0 & 0 & 0 \\ J_{21}^{(0)} & J_{22}^{(1)} & 0 & 0 \\ J_{31}^{(0)} & J_{32}^{(1)} & J_{33}^{(2)} & 0 \\ J_{41}^{(0)} & J_{42}^{(1)} & J_{43}^{(2)} & J_{44}^{(3)} \end{bmatrix} \begin{bmatrix} 1 & J_{12}^{(1)} & J_{13}^{(1)} & J_{14}^{(1)} \\ 0 & 1 & J_{23}^{(2)} & J_{24}^{(2)} \\ 0 & 0 & 1 & J_{34}^{(3)} \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

3.We get : $\boldsymbol{L^k\ U^k\ \Delta v^k = -f(\ v^k)}$

4.Substituting by $\boldsymbol{x^k}$: $\boldsymbol{x^k = U^k\ \Delta v^k}$

5.We first solve the lower triangular matrix by **Forward Substitution :**

$$\boldsymbol{L^k\ x^k = -f(\ v^k)}$$

6.Solve the upper triangular matrix by **Back Substitution** to get $\Delta \boldsymbol{v}$ **:**

$$\boldsymbol{U^k\ \Delta v^k\ = x^k}$$

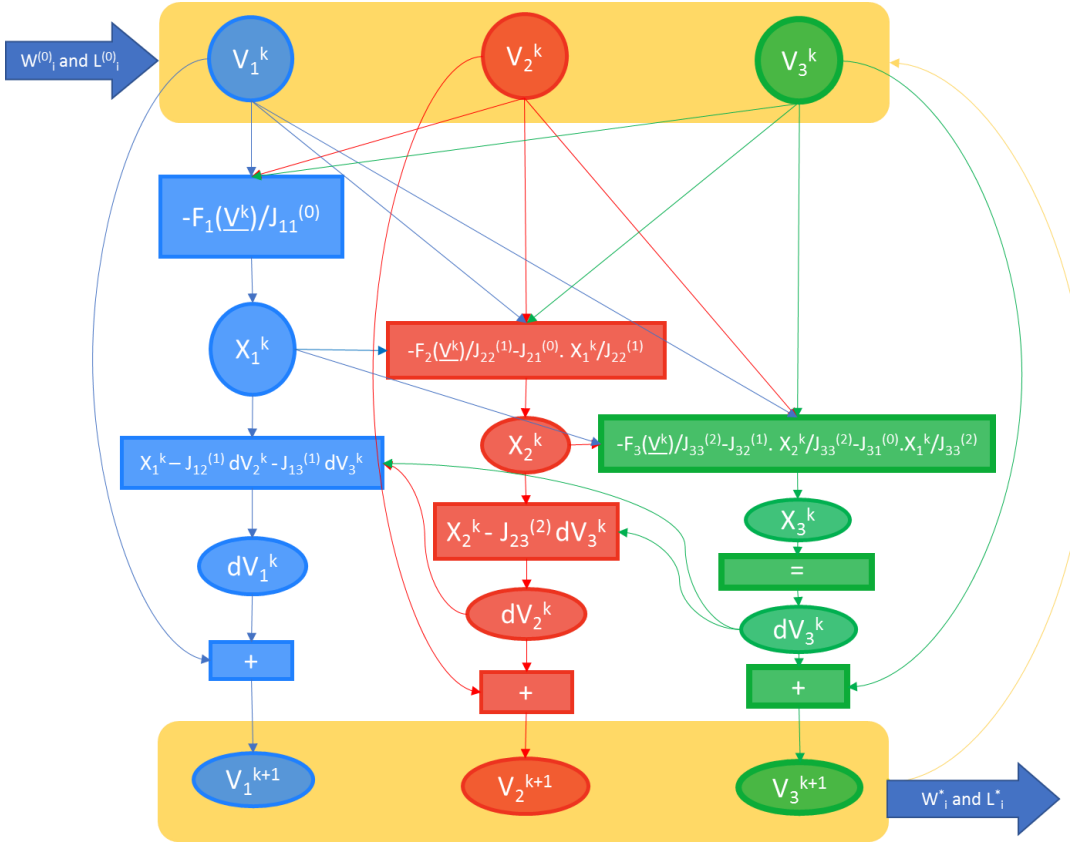
7.Finally, we update current variables **:**

$$\boldsymbol{v^{k+1} = v^k + \Delta v^k}$$

Graph Representation of DC Nonlinear Equations

Simultaneous Resolution in Spice:

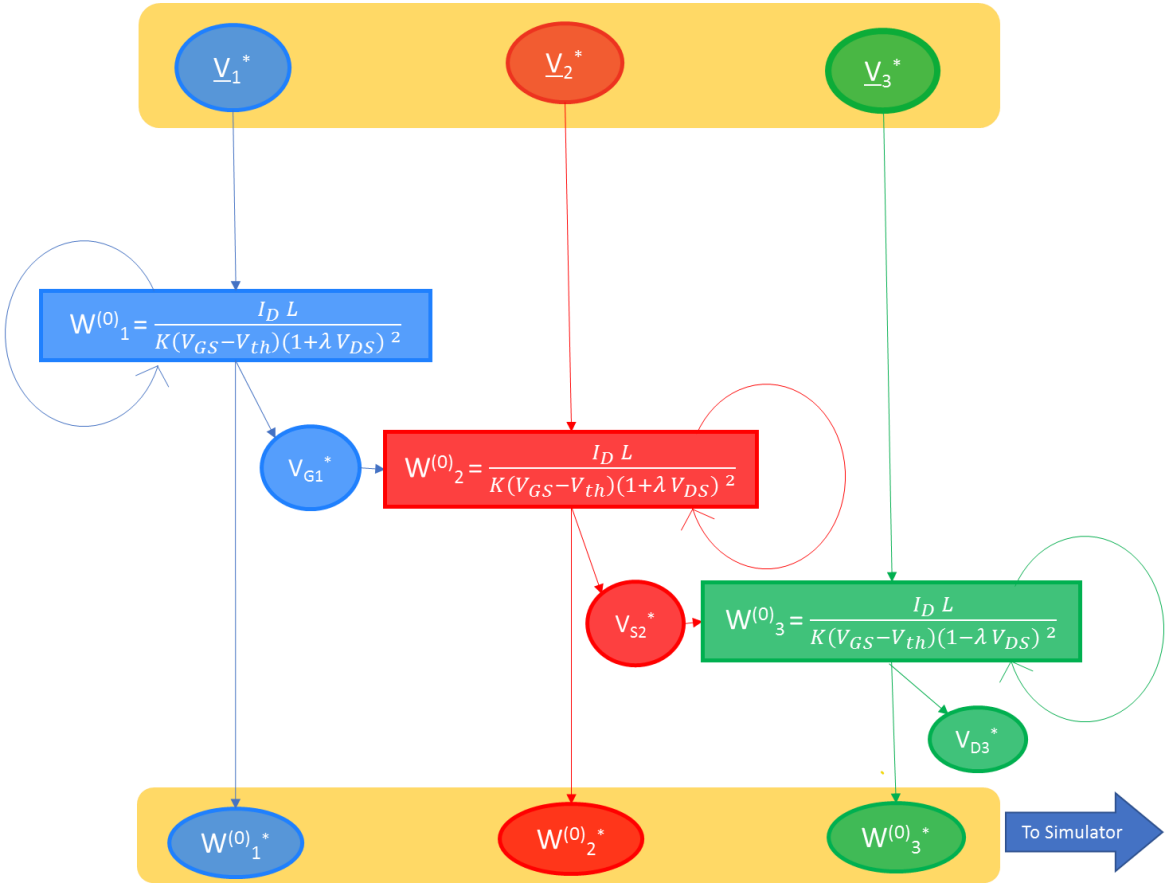
- Matrix–based formulation
- Each iteration requires large number of computations
- Spice model of computation is complex
- Jacobian computation becomes a major component
- Does not follow human design perception



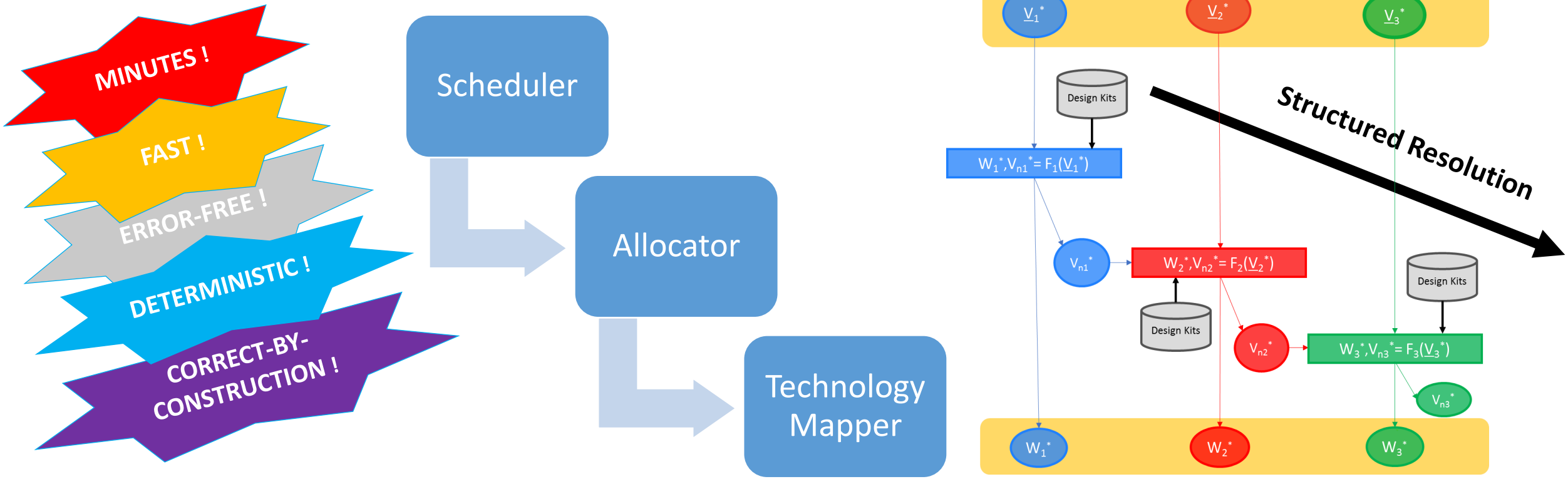
Human Perception for Analog Design

Structured Resolution :

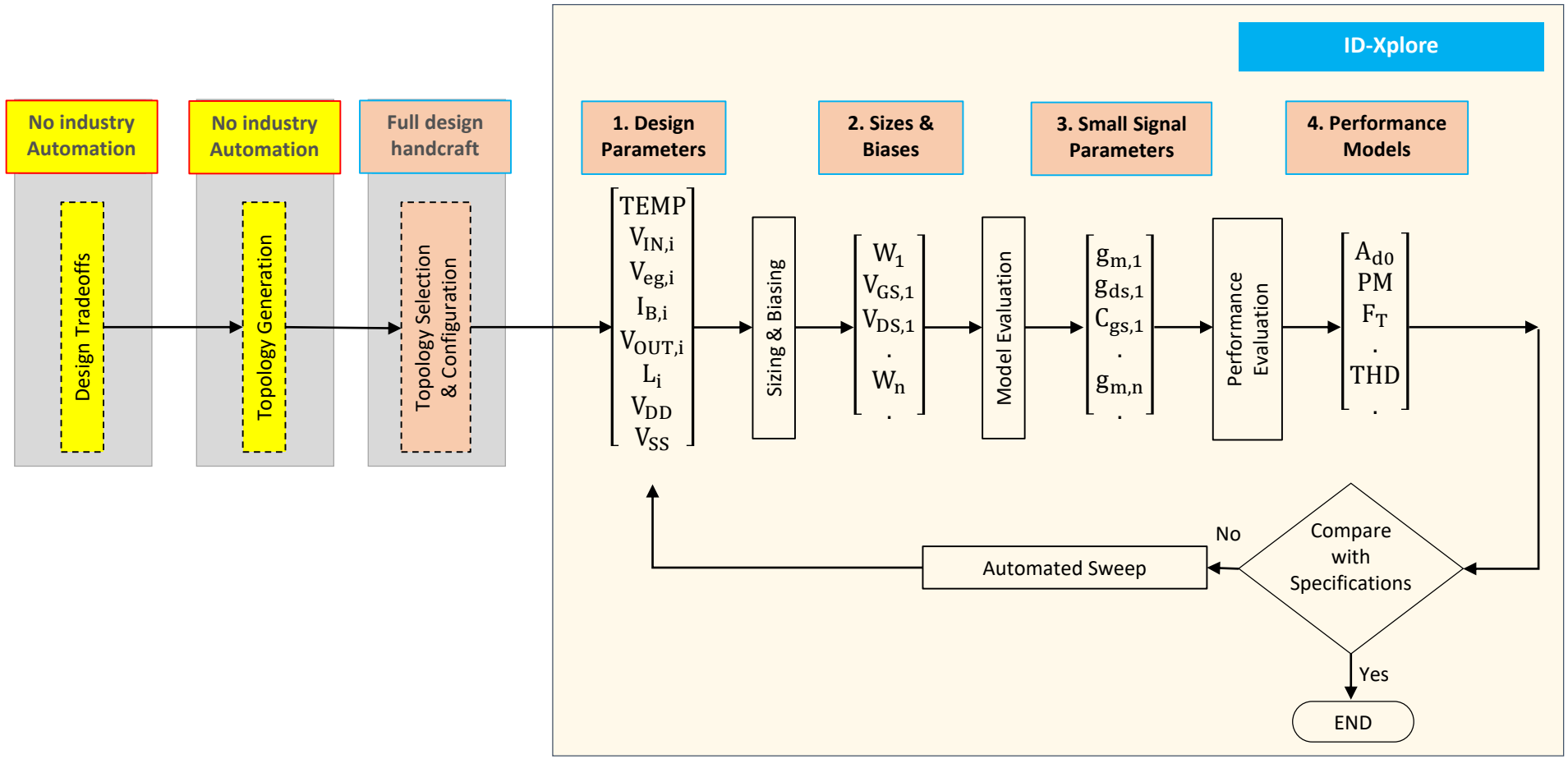
- No matrix–based formulation
- Each iteration requires only one computation
- Model of computation becomes very simple
- Jacobian computation almost disappears
- Follows well human design perception
- Not easily automatable.



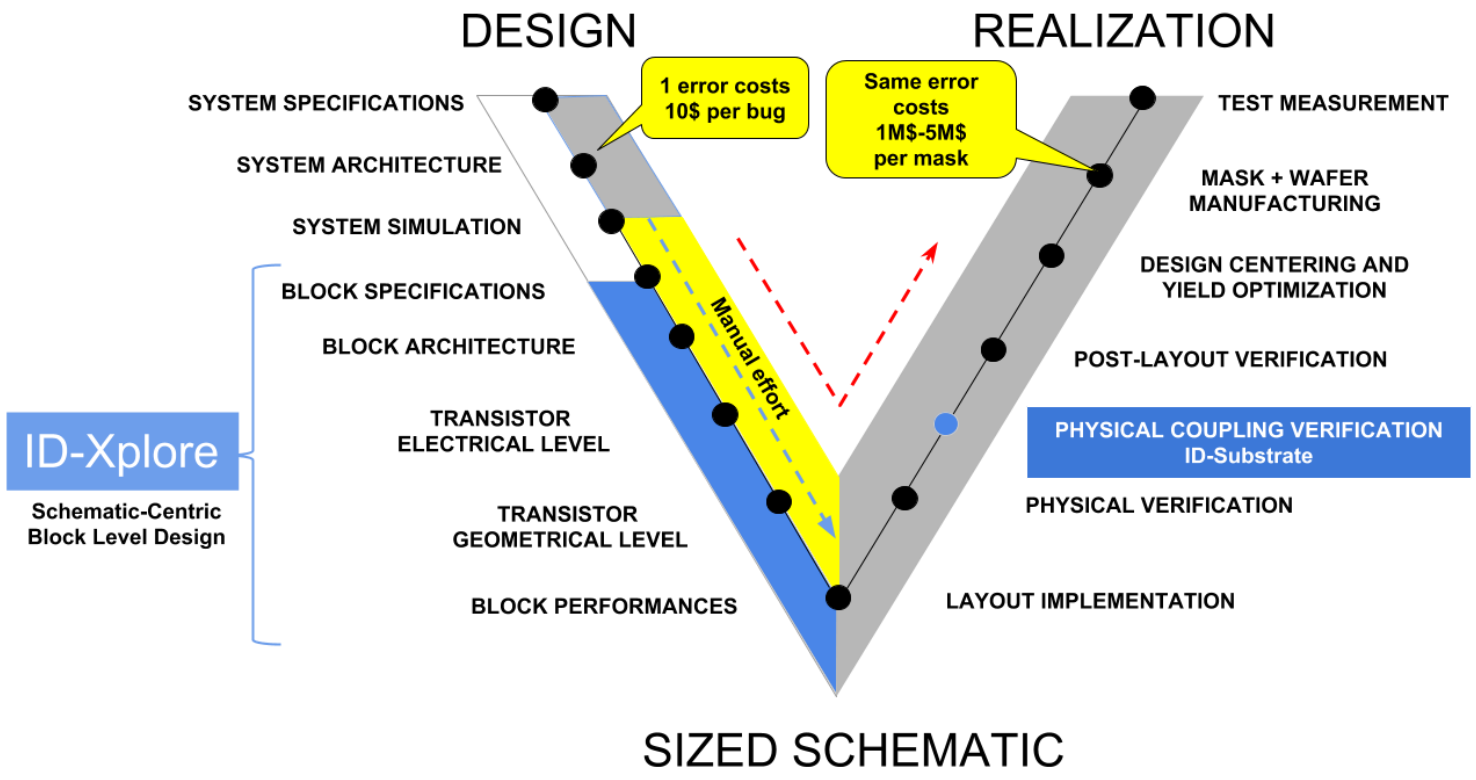
Intento Design Digitally-Inspired Analog Solver



Intento Design Product Defintion for ID-Xplore™



From Block Specification to Performance



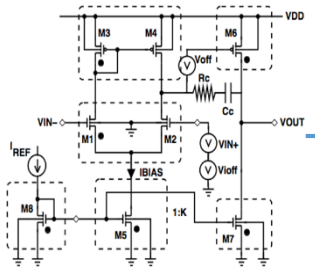
✓ **Shorten productivity gap**

✓ **Shorten quality gap**

✓ **Avoid design respins**

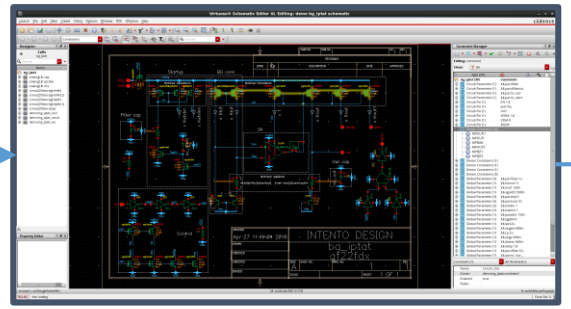
Intento Design Cognitive Front-End Design & Migration Tool

Schematic



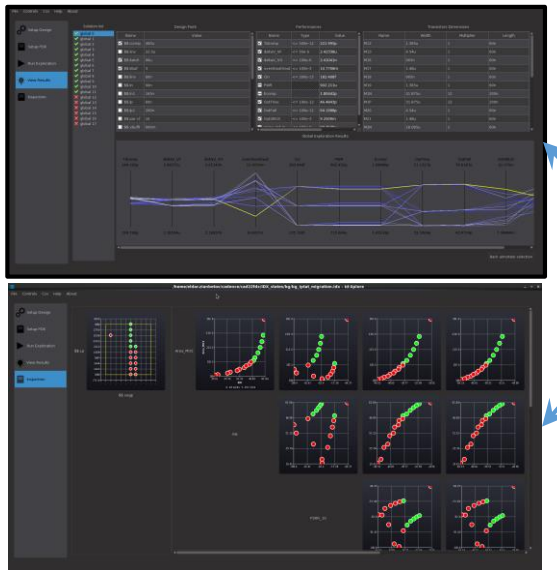
Human Tacit Knowledge

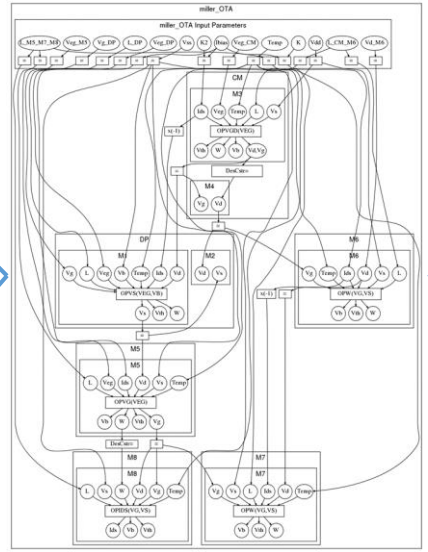
Tacit-to-Formal



Schematic XL Constraint Manager

Tacit & Formal Knowledge in OpenAccess DB



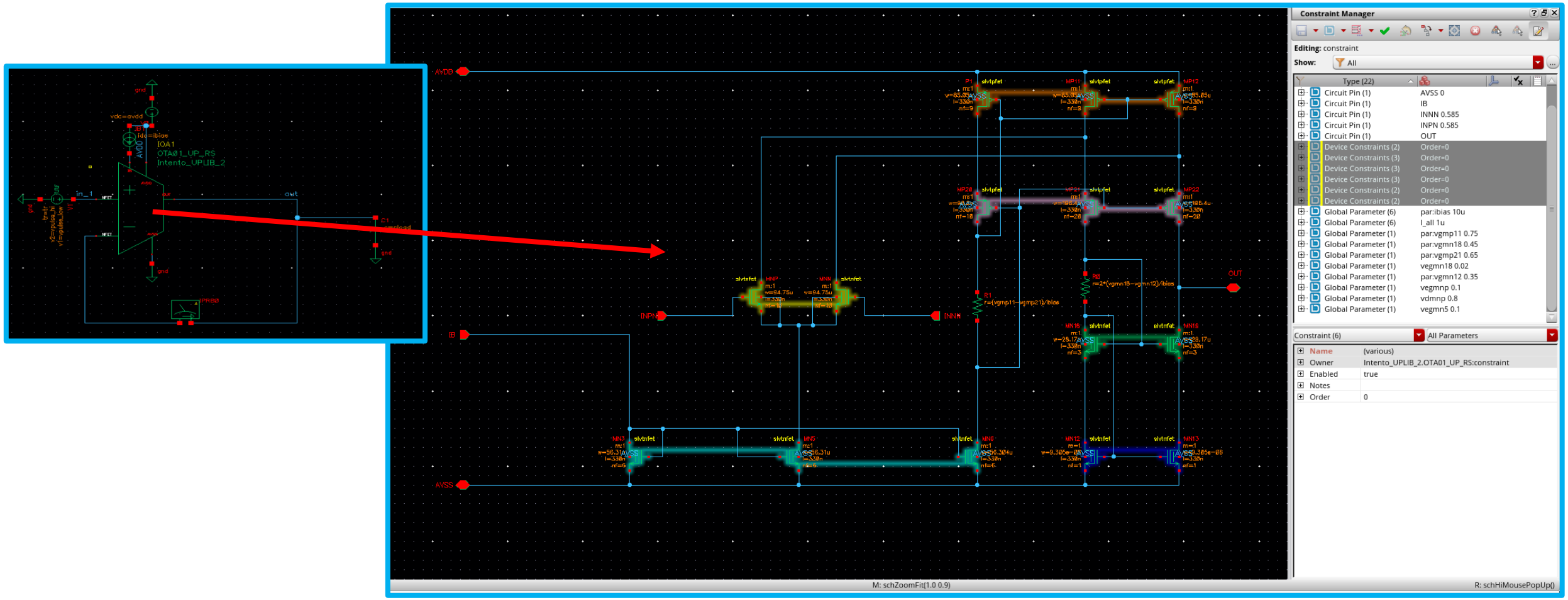


Structured Design Representation

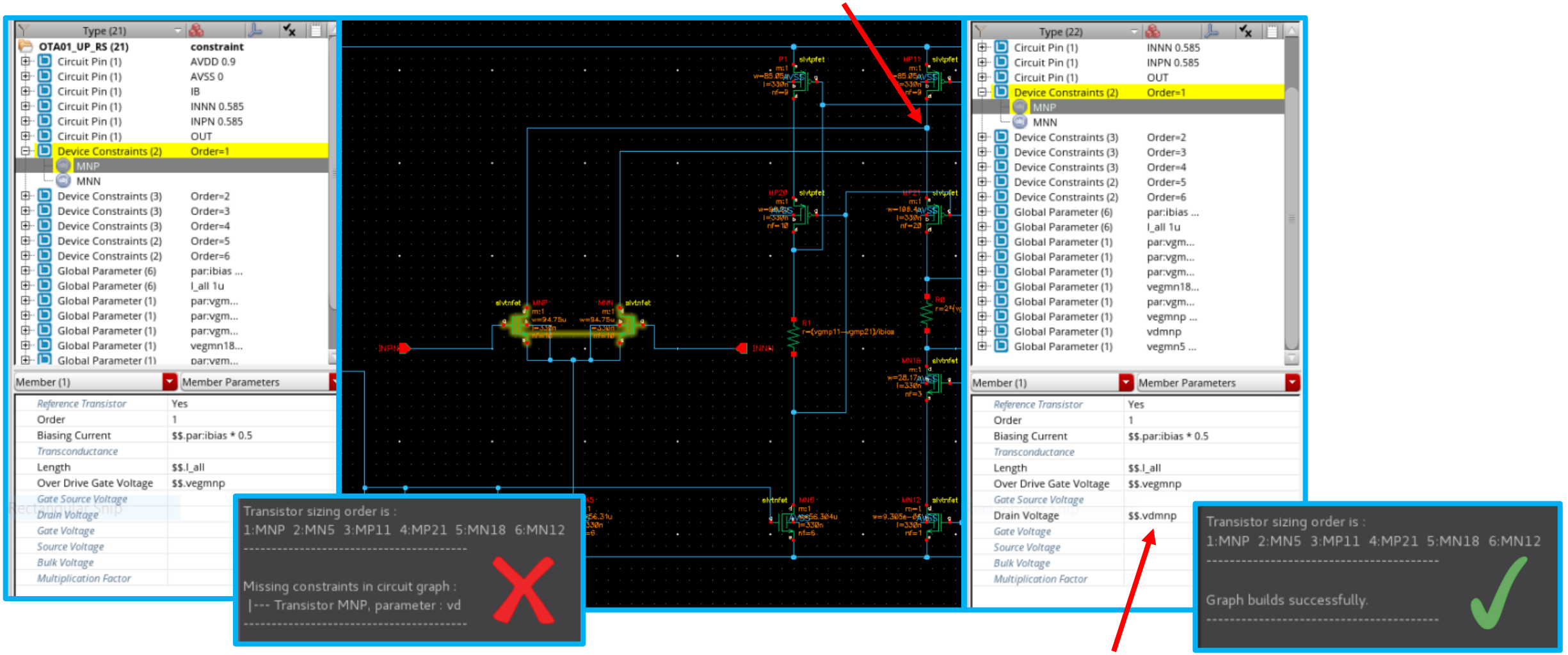
Verification of Human Reasoning in the Analog Design

XPLORE

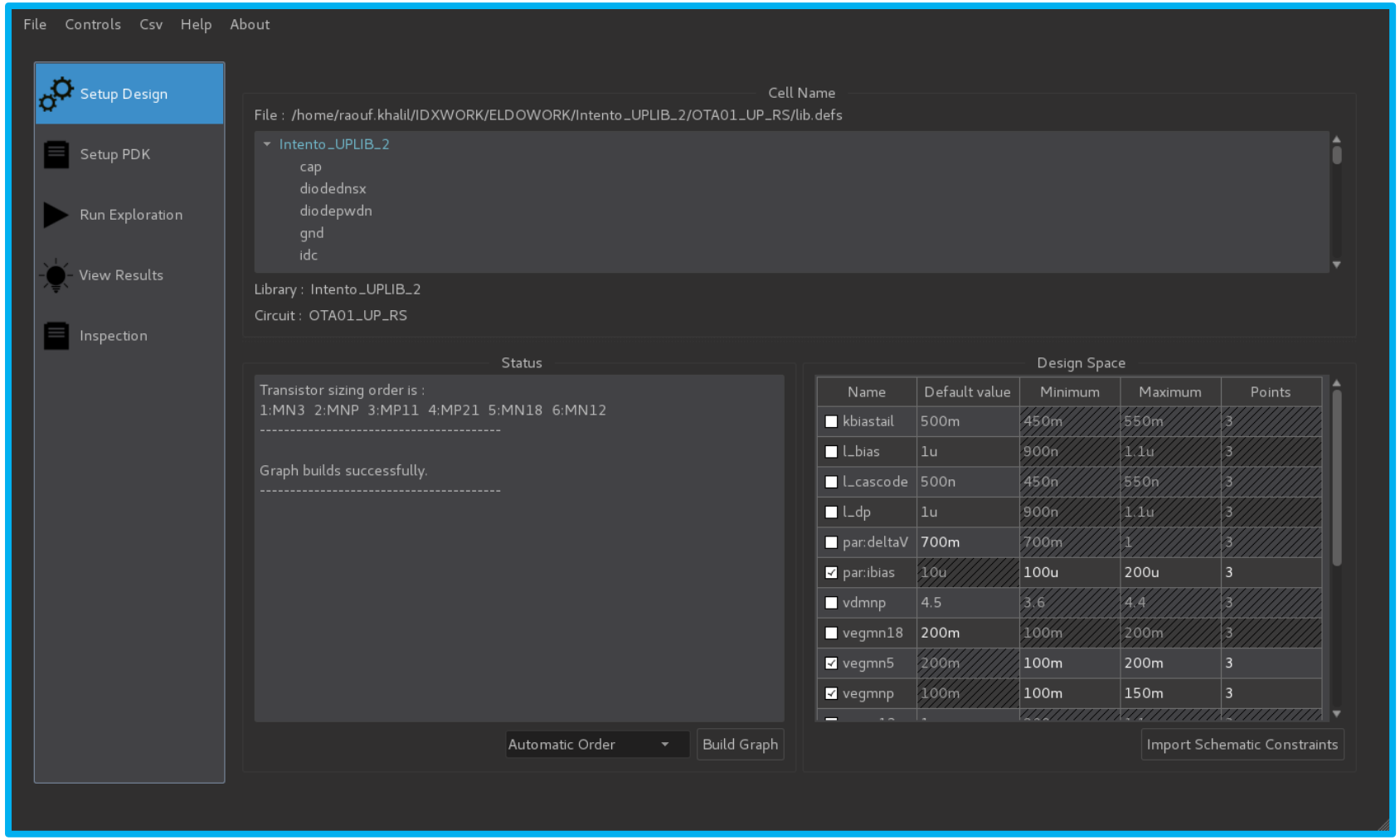
Constraint Manager: Tacit to Formal Knowledge



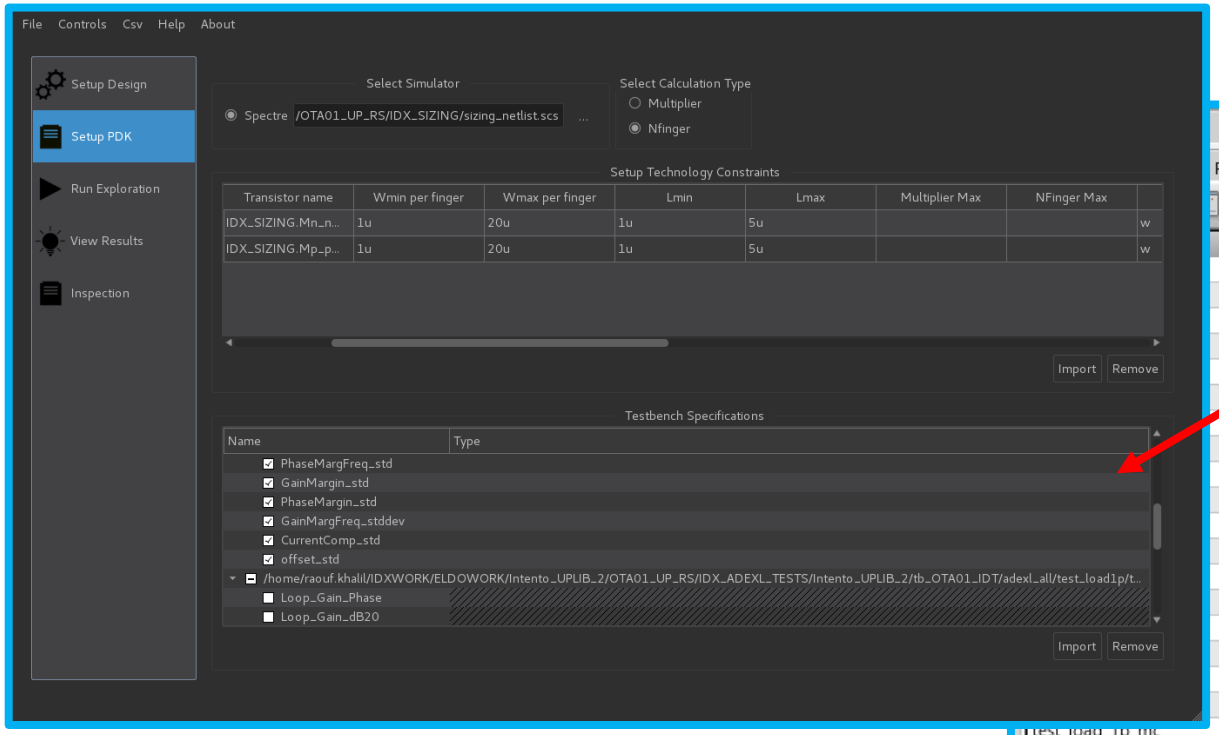
Verification of Human Reasoning in the Analog Design

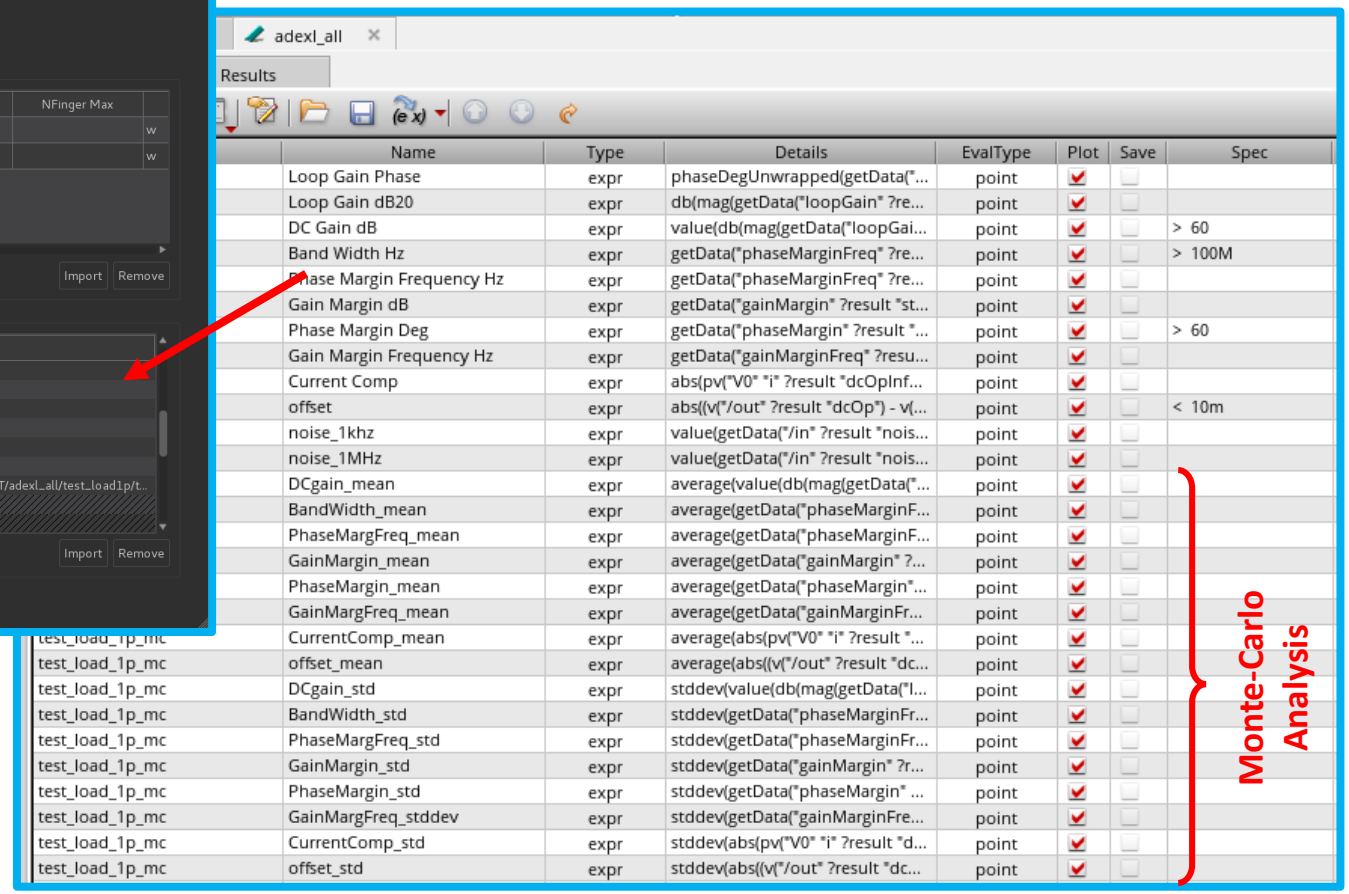


Setup Design Space for AMS 0.35µm with V_{DD} = 5V

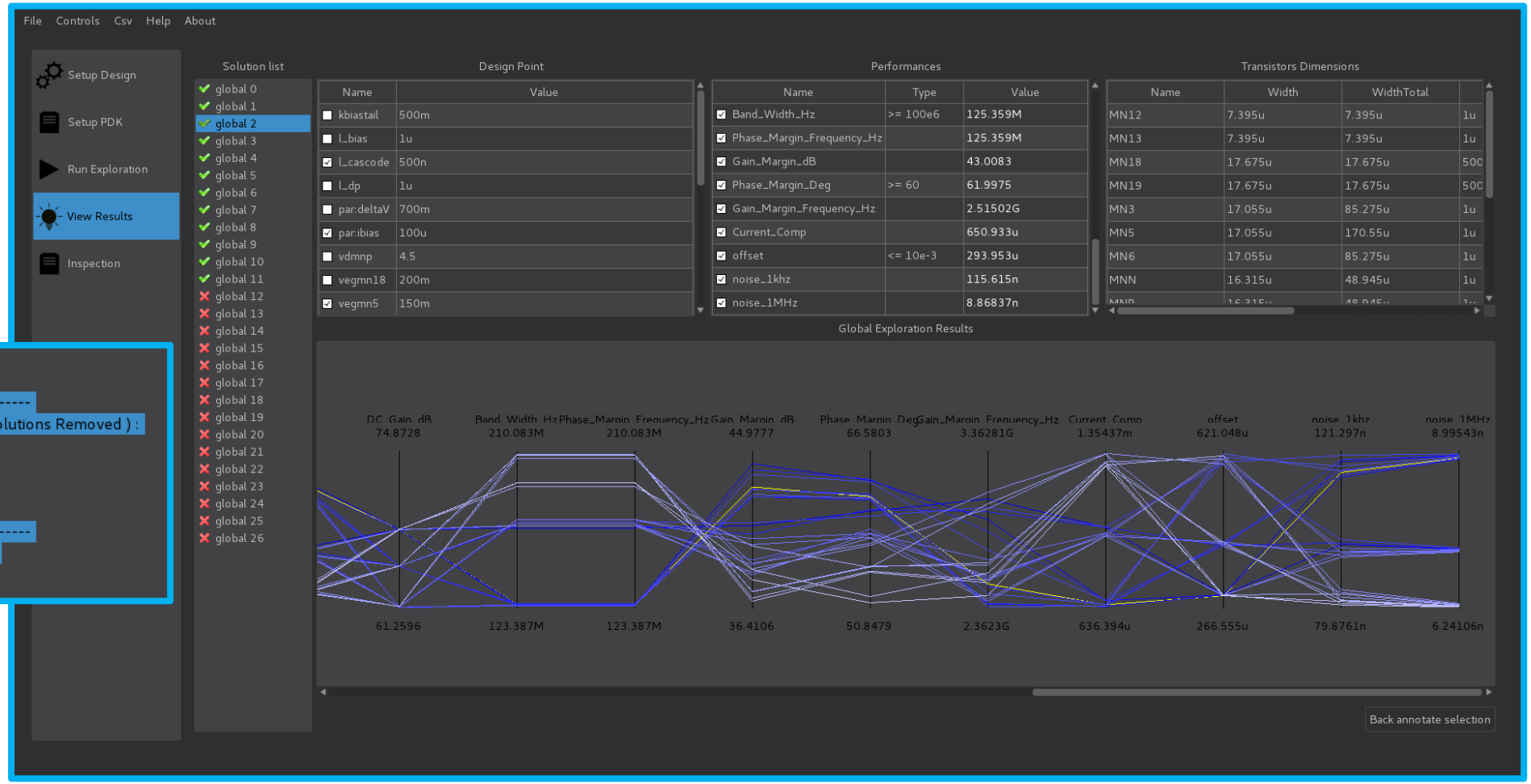


Setup Design Space for AMS 0.35µm with V_{DD} = 5V





View Design Tradeoffs for AMS 0.35µm with V_{DD} = 5V



Inspect Design Space for AMS 0.35µm with V_{DD} = 5V

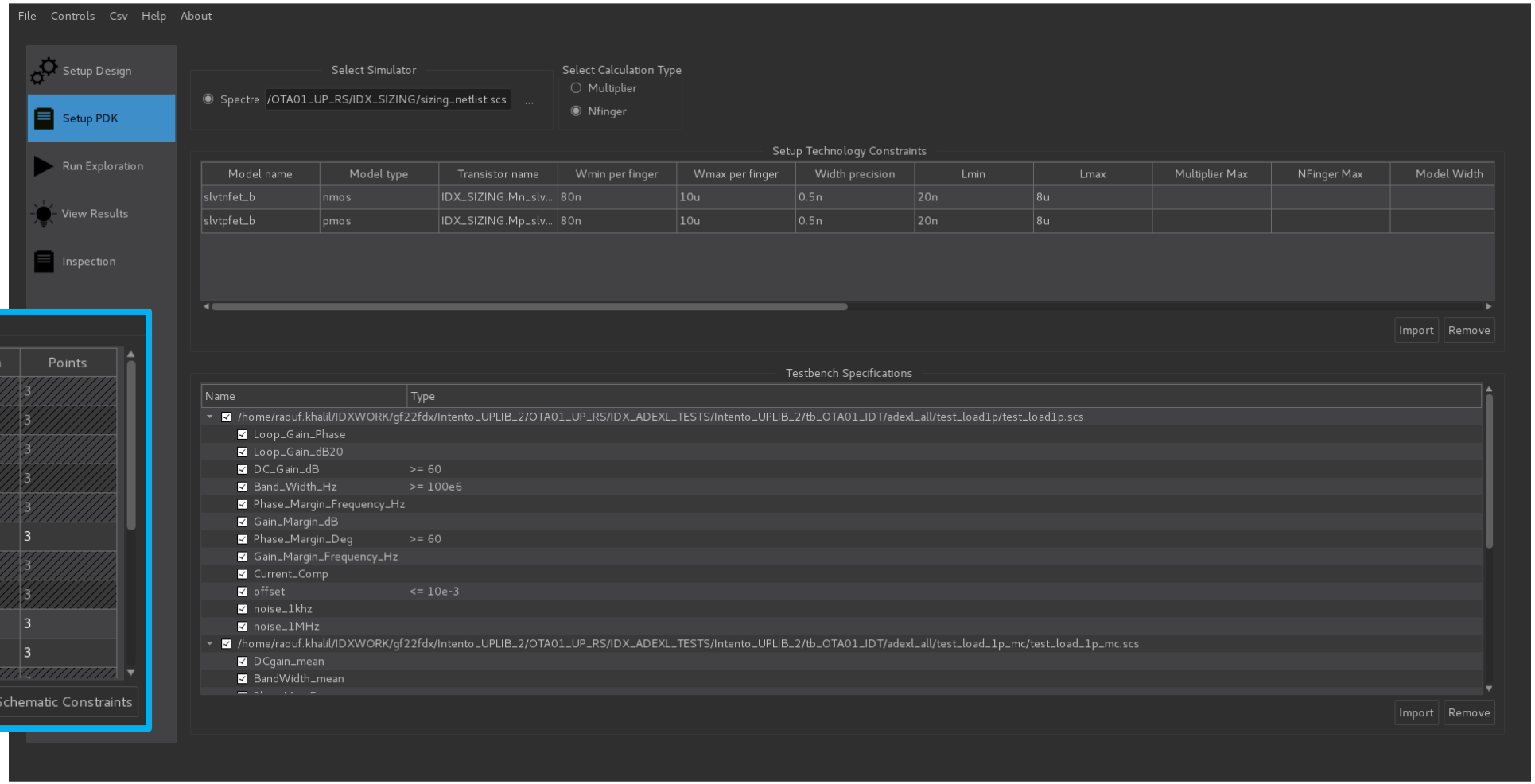
Front-End Signoff Simulation with ADE-Assembler for AMS 0.35µm with V_{DD} = 5V

Test	Output	Nominal	Spec	Weight	Pass/Fail
test_load_1p_mc	DCgain_mean	67.95			
test_load_1p_mc	BandWidth_mean	124.9M			
test_load_1p_mc	PhaseMargFreq...	124.9M			
test_load_1p_mc	GainMargin_me...	43.09			
test_load_1p_mc	PhaseMargin_m...	62.04			
test_load_1p_mc	GainMargFreq_...	2.536G			
test_load_1p_mc	CurrentComp_...	651.7u			
test_load_1p_mc	offset_mean	2.314m			
test_load_1p_mc	DCgain_std	1.316			
test_load_1p_mc	BandWidth_std	3.392M			
test_load_1p_mc	PhaseMargFreq...	3.392M			
test_load_1p_mc	GainMargin_std	443.6m			
test_load_1p_mc	PhaseMargin_std	929m			
test_load_1p_mc	GainMargFreq_s...	105M			
test_load_1p_mc	CurrentComp_std	9.851u			
test_load_1p_mc	offset_std	1.68m			
test_load1p	Loop Gain Phase				
test_load1p	Loop Gain dB20				
test_load1p	DC Gain dB	68.06	> 60		pass
test_load1p	Band Width Hz	125.3M	> 100M		pass
test_load1p	Phase Margin Fr...	125.3M			
test_load1p	Gain Margin dB	43.2			
test_load1p	Phase Margin Deg	62.13	> 60		pass
test_load1p	Gain Margin Fre...	2.565G			
test_load1p	Current Comp	653.3u			
test_load1p	offset	293.7u	< 10m		pass
test_load1p	noise_1khz	116n			
test_load1p	noise_1MHz	8.874n			

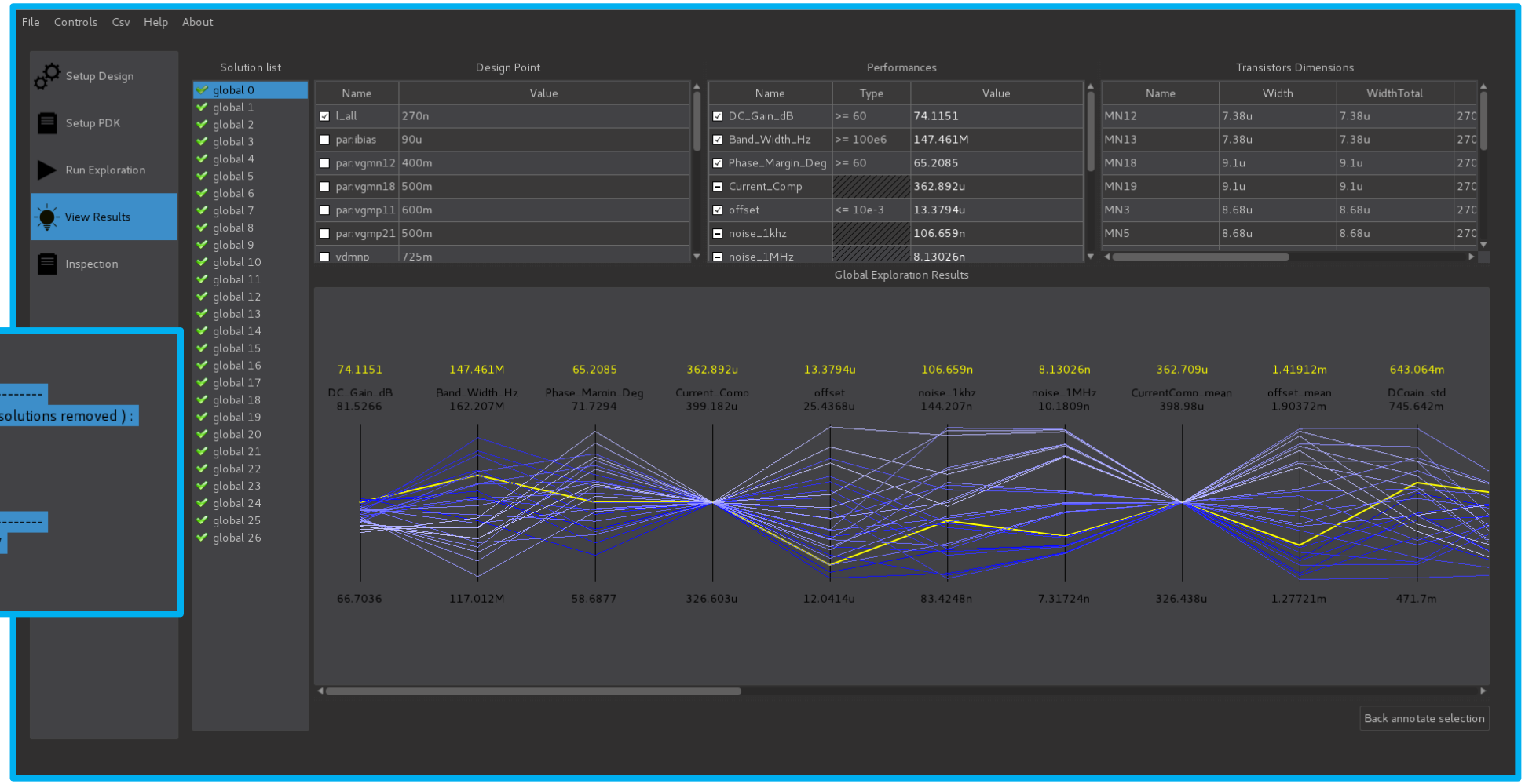
Performances

Name	Type	Value
DCgain_mean		67.9459
BandWidth_mean		124.935M
PhaseMargFreq_mean		124.935M
GainMargin_mean		43.0852
PhaseMargin_mean		62.0364
GainMargFreq_mean		2.53605G
CurrentComp_mean		651.686u
offset_mean		2.31437m
DCgain_std		1.31612
BandWidth_std		3.3924M
PhaseMargFreq_std		3.3924M
GainMargin_std		443.592m
PhaseMargin_std		929.035m
GainMargFreq_stddev		105.042M
CurrentComp_std		9.85083u
offset_std		1.67999m
DC_Gain_dB	>= 60	68.0559
Band_Width_Hz	>= 100e6	125.332M
Phase_Margin_Frequency_Hz		125.332M
Gain_Margin_dB		43.2011
Phase_Margin_Deg	>= 60	62.1335
Gain_Margin_Frequency_Hz		2.56543G
Current_Comp		653.27u
offset	<= 10e-3	293.733u
noise_1khz		115.977n

Setup Design Space and PDK For Migration to GF 22nm FDX with V_{DD} = 1.2V

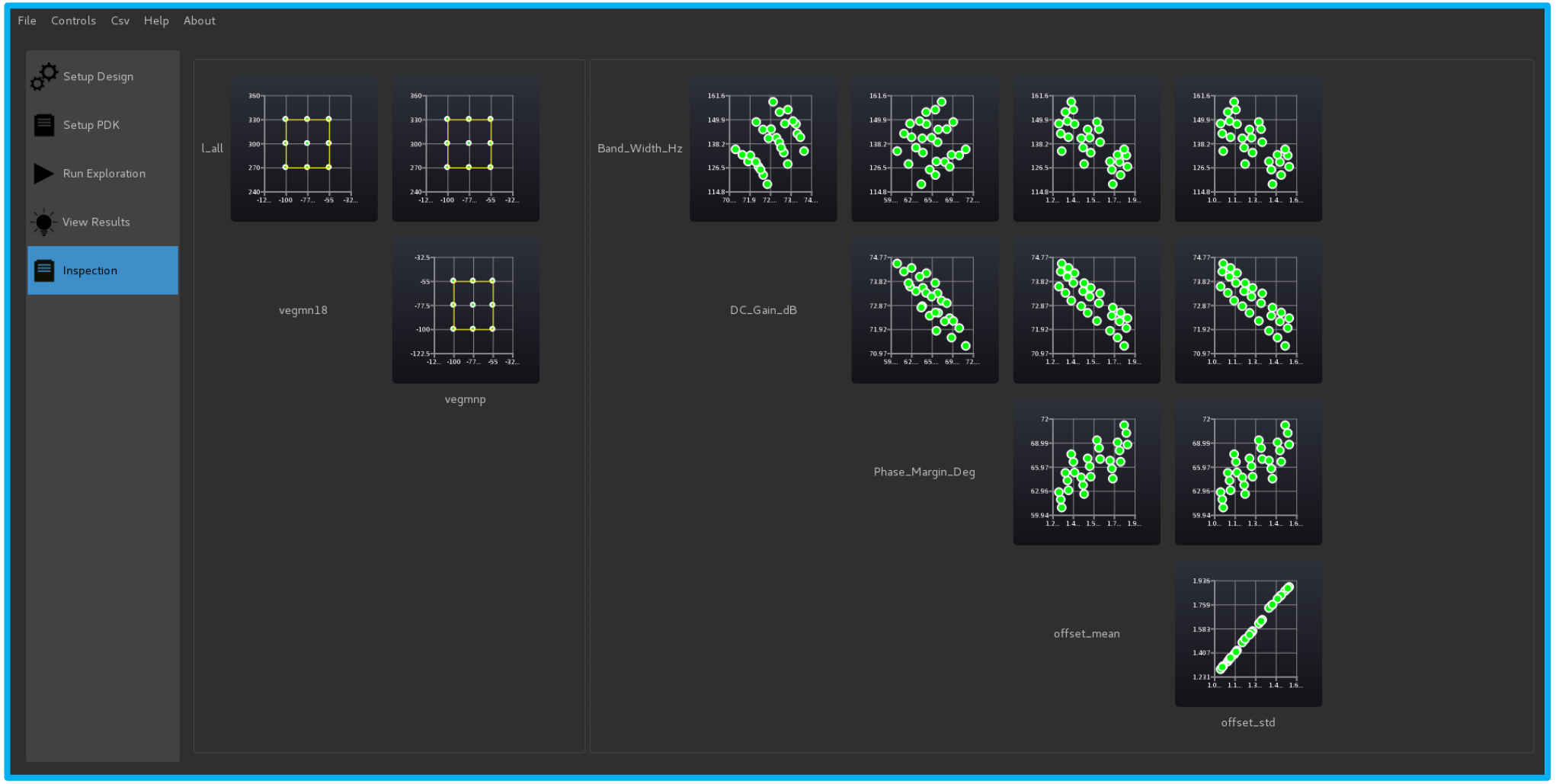


View Design Tradeoffs for GF 22nm FDX with V_{DD} = 1.2V




```
TOTAL DURATION :  404.173 seconds.
-------------------------------------------------------------------------
SUMMARY OF THE EVALUATED SOLUTIONS ( 0 duplicate solutions removed ) :
        27    VALID
        0     SOFT VALID
        0     INVALID
        0     NOT EVALUATED
-------------------------------------------------------------------------
The number of calls in parallelized Peano exploration is : 27
 ==== END of parallelized Peano exploration ====
```

Inspect Migration Space for GF 22nm FDX with V_{DD} = 1.2V



Front-End Signoff Simulation for GF 22nm FDX with V_{DD} = 1.2V

Test	Output	Nominal	Spec	Weight	Pass/Fail
test_load1p	Loop Gain Phase				
test_load1p	Loop Gain dB20				
test_load1p	DC Gain dB	69.03	> 60		pass
test_load1p	Band Width Hz	212.6M	> 100M		pass
test_load1p	Phase Margin Fr...	212.6M			
test_load1p	Gain Margin dB	27.73			
test_load1p	Phase Margin Deg	67.35	> 60		pass
test_load1p	Gain Margin Fre...	1.855G			
test_load1p	Current Comp	607.3u			
test_load1p	offset	35.55u	< 10m		pass
test_load1p	noise_1khz	114.8n			
test_load1p	noise_1MHz	8.038n			
test_load_1p_mc	DCgain_mean	69			
test_load_1p_mc	BandWidth_mean	212.8M			
test_load_1p_mc	PhaseMargFreq...	212.8M			
test_load_1p_mc	GainMargin_me...	27.74			
test_load_1p_mc	PhaseMargin_m...	67.35			
test_load_1p_mc	GainMargFreq_...	1.86G			
test_load_1p_mc	CurrentComp_...	607u			
test_load_1p_mc	offset_mean	1.498m			
test_load_1p_mc	DCgain_std	343.6m			
test_load_1p_mc	BandWidth_std	3.426M			
test_load_1p_mc	PhaseMargFreq...	3.426M			
test_load_1p_mc	GainMargin_std	586.3m			
test_load_1p_mc	PhaseMargin_std	555.8m			
test_load_1p_mc	GainMargFreq_s...	90.27M			
test_load_1p_mc	CurrentComp_std	8.895u			
test_load_1p_mc	offset_std	1.22m			

Performances

Name	Type	Value
DC_Gain_dB	>= 60	69.0346
Band_Width_Hz	>= 100e6	212.823M
Phase_Margin_Frequency_Hz		212.823M
Gain_Margin_dB		27.4937
Phase_Margin_Deg	>= 60	67.1791
Gain_Margin_Frequency_Hz		1.82981G
Current_Comp		607.258u
offset	<= 10e-3	35.5514u
noise_1khz		114.838n
noise_1MHz		8.03795n
DCgain_mean		69.0025
BandWidth_mean		213.09M
PhaseMargFreq_mean		213.09M
GainMargin_mean		27.4984
PhaseMargin_mean		67.1773
GainMargFreq_mean		1.83483G
CurrentComp_mean		606.979u
offset_mean		1.49838m
DCgain_std		343.577m
BandWidth_std		3.43186M
PhaseMargFreq_std		3.43186M
GainMargin_std		585.76m
PhaseMargin_std		560.974m
GainMargFreq_stddev		89.9229M
CurrentComp_std		8.89481u

Summary

- ✓ ID-Xplore™ is the first industrial cognitive software for very fast analog design and migration of analog IP
- ✓ It is used to produce first-time right analog IP
- ✓ Cognitive means mimicing human design reasoning
- ✓ The Digital transformation shall promote « Cognitive EDA » versus « Traditional EDA »
- ✓ Cognitive EDA will drastically boost design productivity, production quality and time-to-market by at least two order of magnitudes.
- ✓ Cognitive EDA will empower human capacity through efficient collaboration with intelligent machines

Thank you for your kind attention.

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