

ID-Xplore™: A Cognitive Software for Designing First-Time Right Analog IP

Dr. Ramy ISKANDER, PhD

Founder & CEO of Intento Design

Email: ramy.iskander@intento-design.com

FR-cell : +33 6 95 25 15 09

US-cell : +1 (408) 514-9871

Hierarchy of Intelligence:

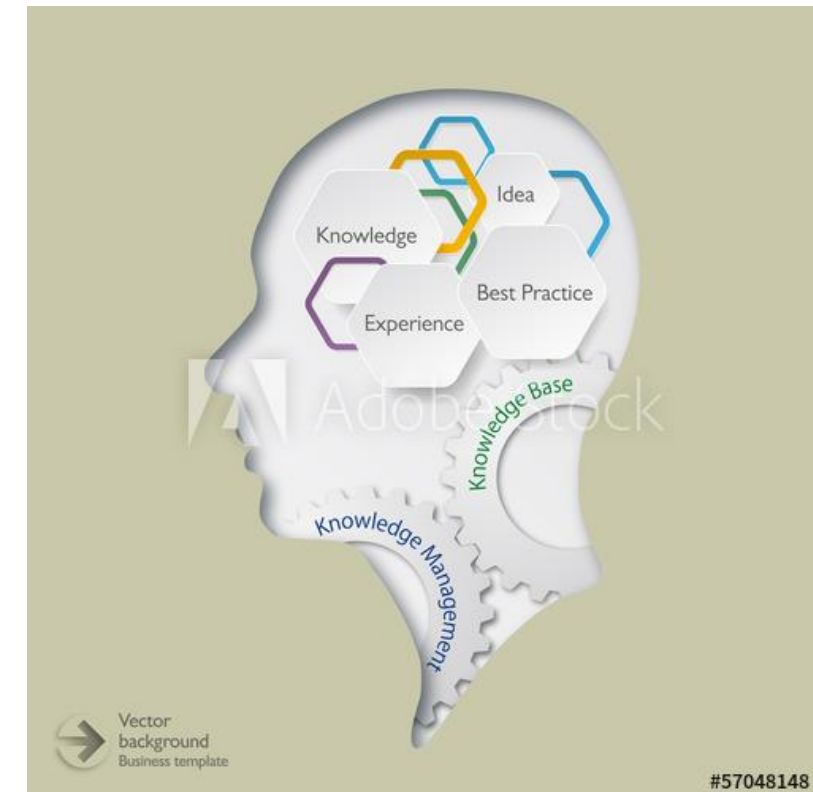
- ☐ **Machine Learning (ML) – We are stuck here !**
Lowest level of data mining and classification
- ☐ **Artificial Intelligence (AI)**
Connect algorithms to perform complex tasks
- ☐ **Cognitive Intelligence (CI)**
Reasoning and building different concepts
in a deterministic and logic manner



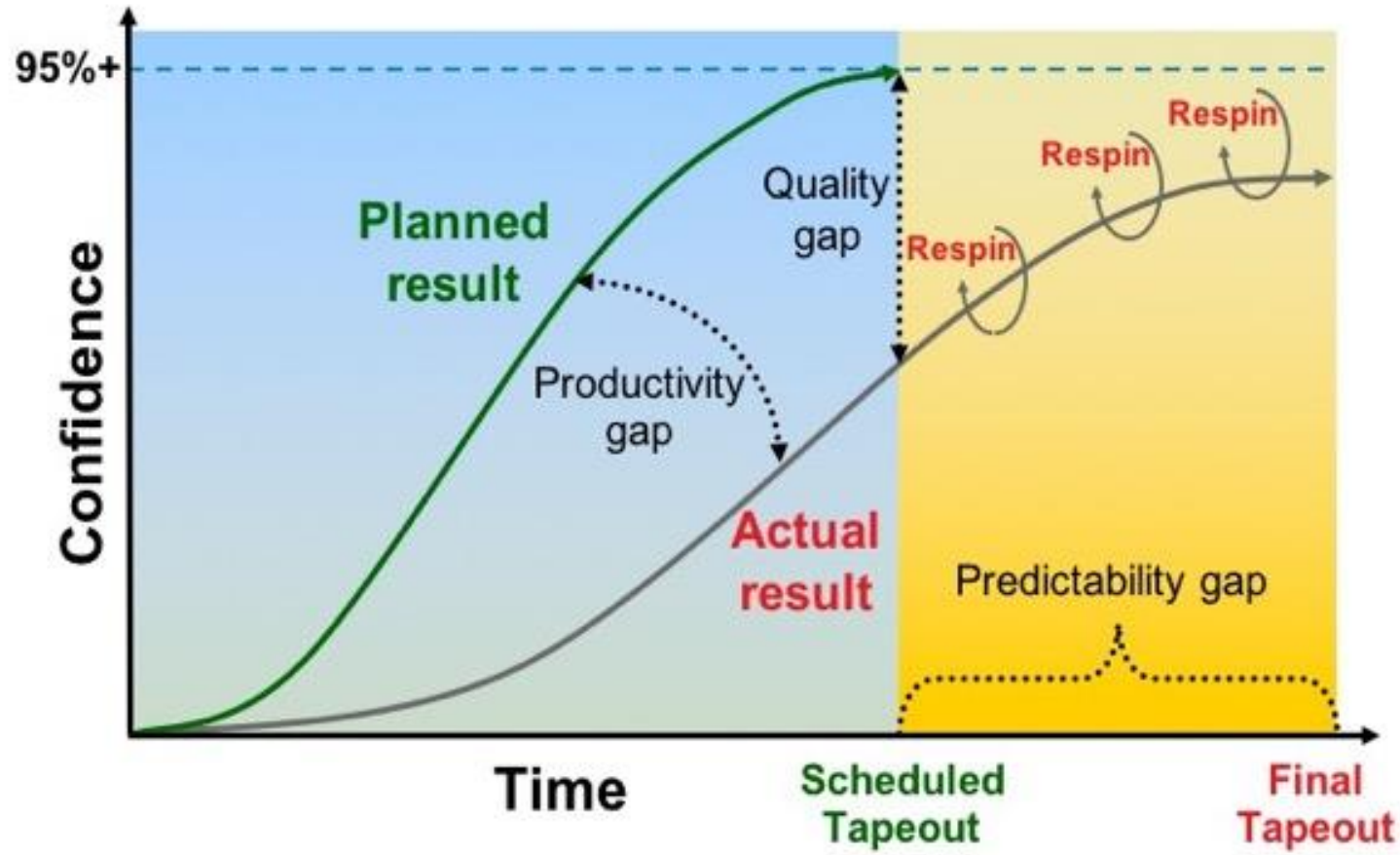
Knowledge can be classified into:

1. **Meta-knowledge:** involves general cultural and philosophical assumptions
2. **Milieu:** is knowledge about the local environment
3. **Tacit knowledge:** is rooted in practice and experience.
4. **Informal knowledge:** is made up of rules of thumb or tricks of the trade
5. **Formal knowledge:** involves theories and proven formulae
6. **Instrumentalities:** embedded in tools and instruments
7. **Contingent knowledge:** is distributed and apparently trivial information specific to a particular environment

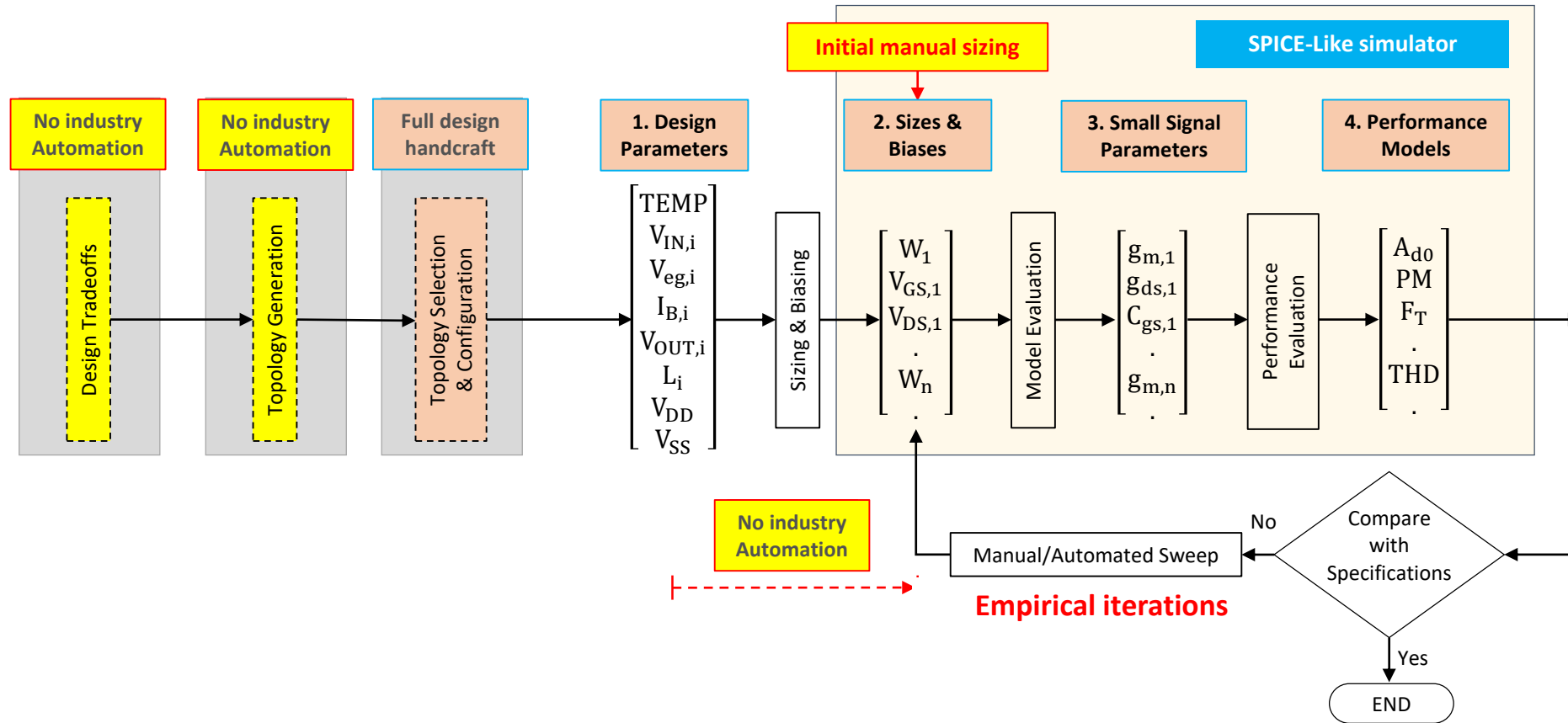
Tacit knowledge



What keeps AMS designers up at night ?



Traditional Analog Design Method



Nonlinear DC Analysis in Spice Simulators

1. From **NR algorithm** : $J^k \Delta v^k = -f(v^k)$

2. From **LU Decomposition**:

$$J \equiv L U \equiv \begin{bmatrix} J_{11}^{(0)} & 0 & 0 & 0 \\ J_{21}^{(0)} & J_{22}^{(1)} & 0 & 0 \\ J_{31}^{(0)} & J_{32}^{(1)} & J_{33}^{(2)} & 0 \\ J_{41}^{(0)} & J_{42}^{(1)} & J_{43}^{(2)} & J_{44}^{(3)} \end{bmatrix} \begin{bmatrix} 1 & J_{12}^{(1)} & J_{13}^{(1)} & J_{14}^{(1)} \\ 0 & 1 & J_{23}^{(2)} & J_{24}^{(2)} \\ 0 & 0 & 1 & J_{34}^{(3)} \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

6. Solve the upper triangular matrix by **Back Substitution** to get Δv :

$$U^k \Delta v^k = x^k$$

7. Finally, we update current variables :

$$v^{k+1} = v^k + \Delta v^k$$

3. We get : $L^k U^k \Delta v^k = -f(v^k)$

4. Substituting by x^k :

$$x^k = U^k \Delta v^k$$

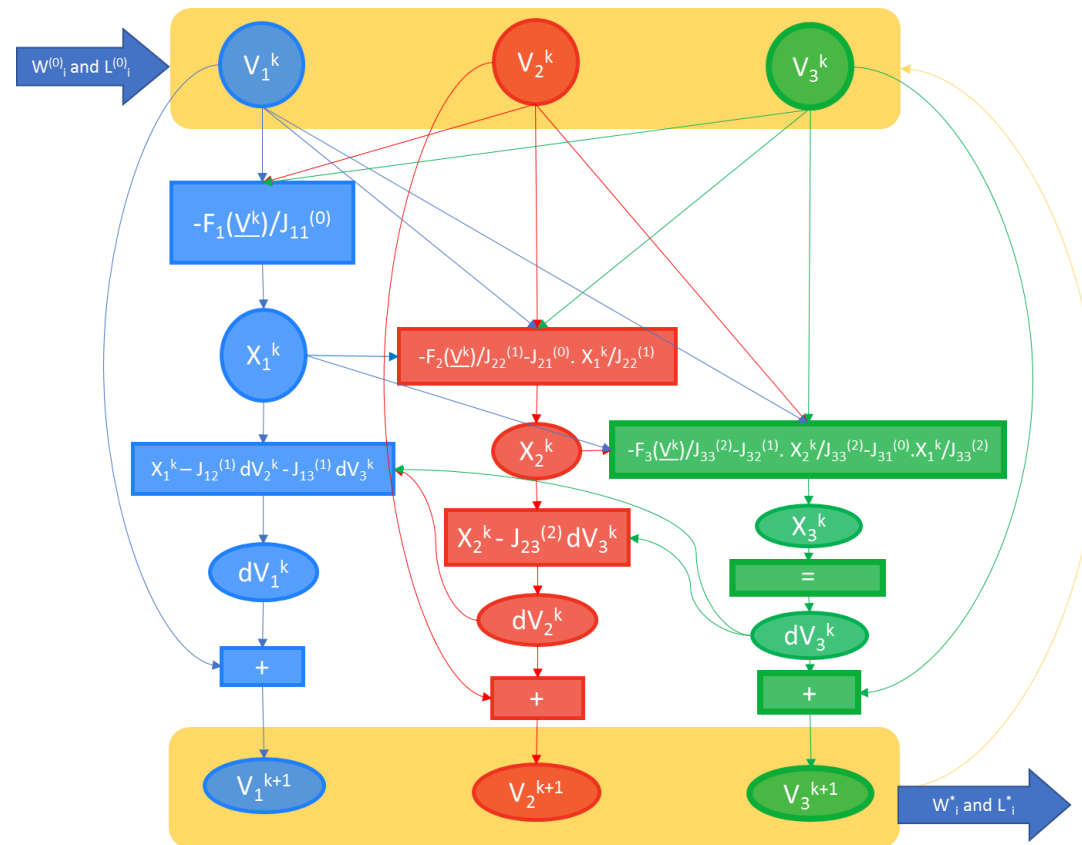
5. We first solve the lower triangular matrix by **Forward Substitution** :

$$L^k x^k = -f(v^k)$$

Graph Representation of DC Nonlinear Equations

Simultaneous Resolution in Spice:

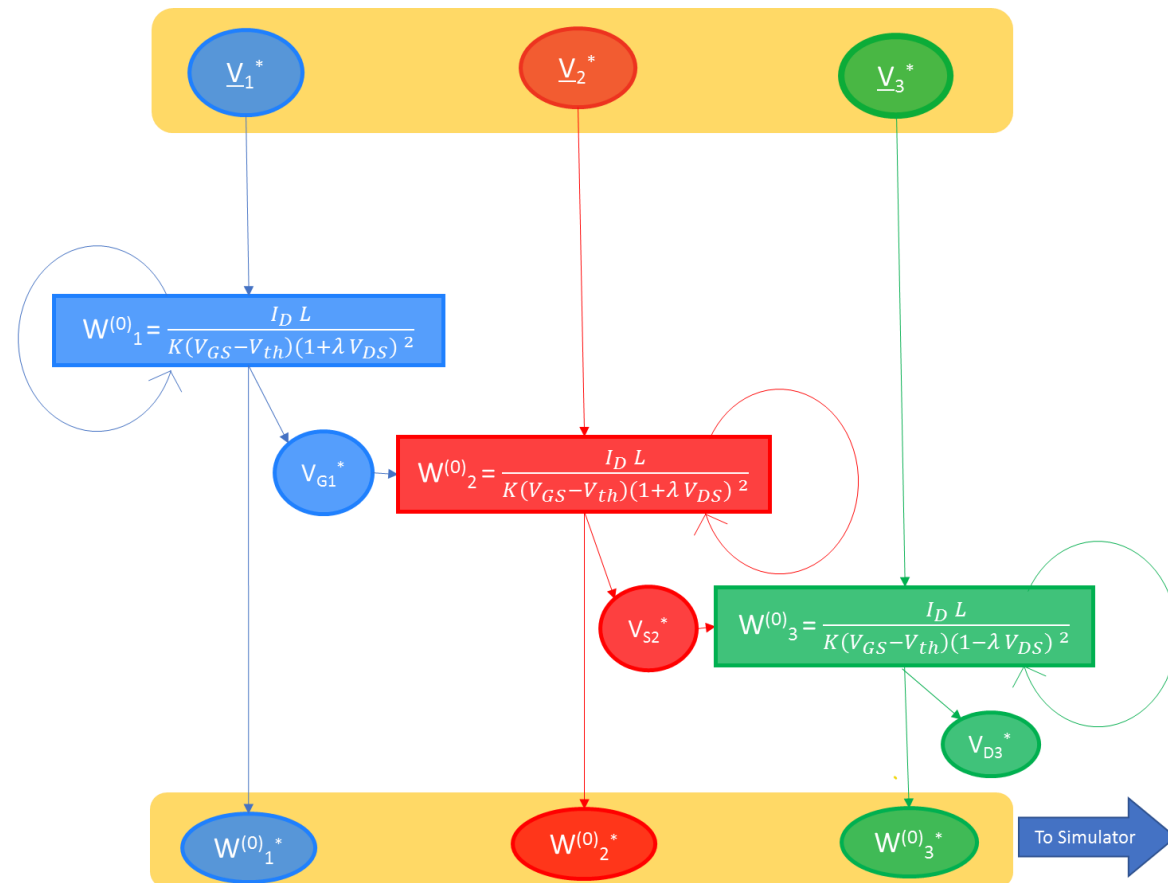
- Matrix-based formulation
- Each iteration requires large number of computations
- Spice model of computation is complex
- Jacobian computation becomes a major component
- Does not follow human design perception



Human Perception for Analog Design

Structured Resolution :

- No matrix-based formulation
- Each iteration requires only one computation
- Model of computation becomes very simple
- Jacobian computation almost disappears
- Follows well human design perception
- Not easily automatable.



Intento Design Digitally-Inspired Analog Solver

MINUTES !

FAST !

ERROR-FREE !

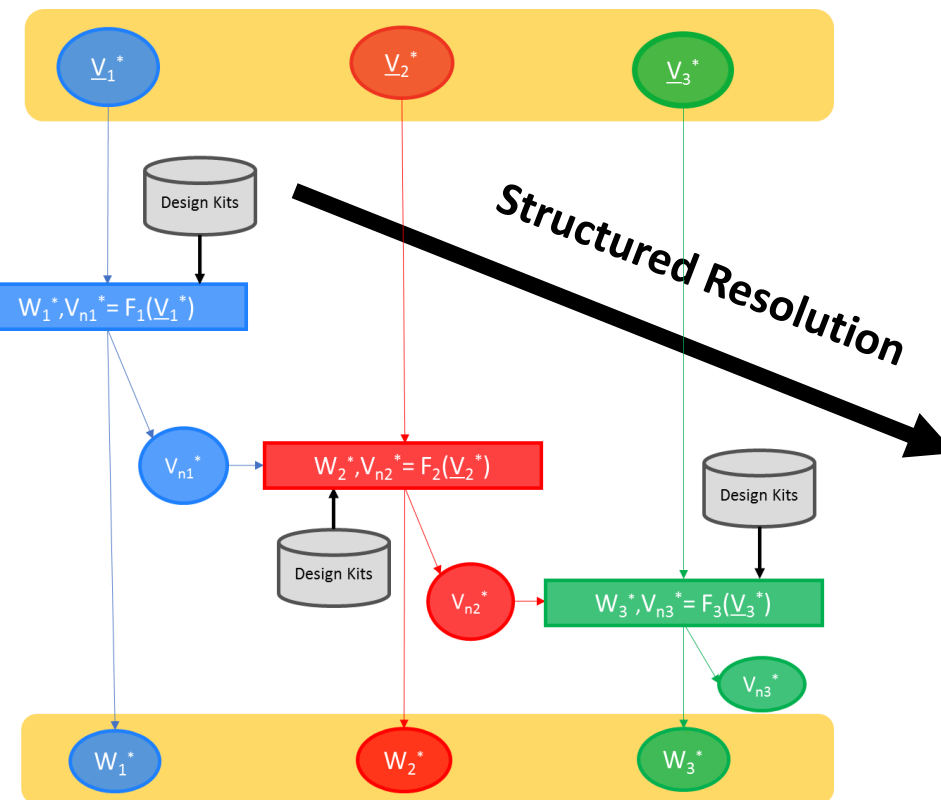
DETERMINISTIC !

CORRECT-BY-CONSTRUCTION !

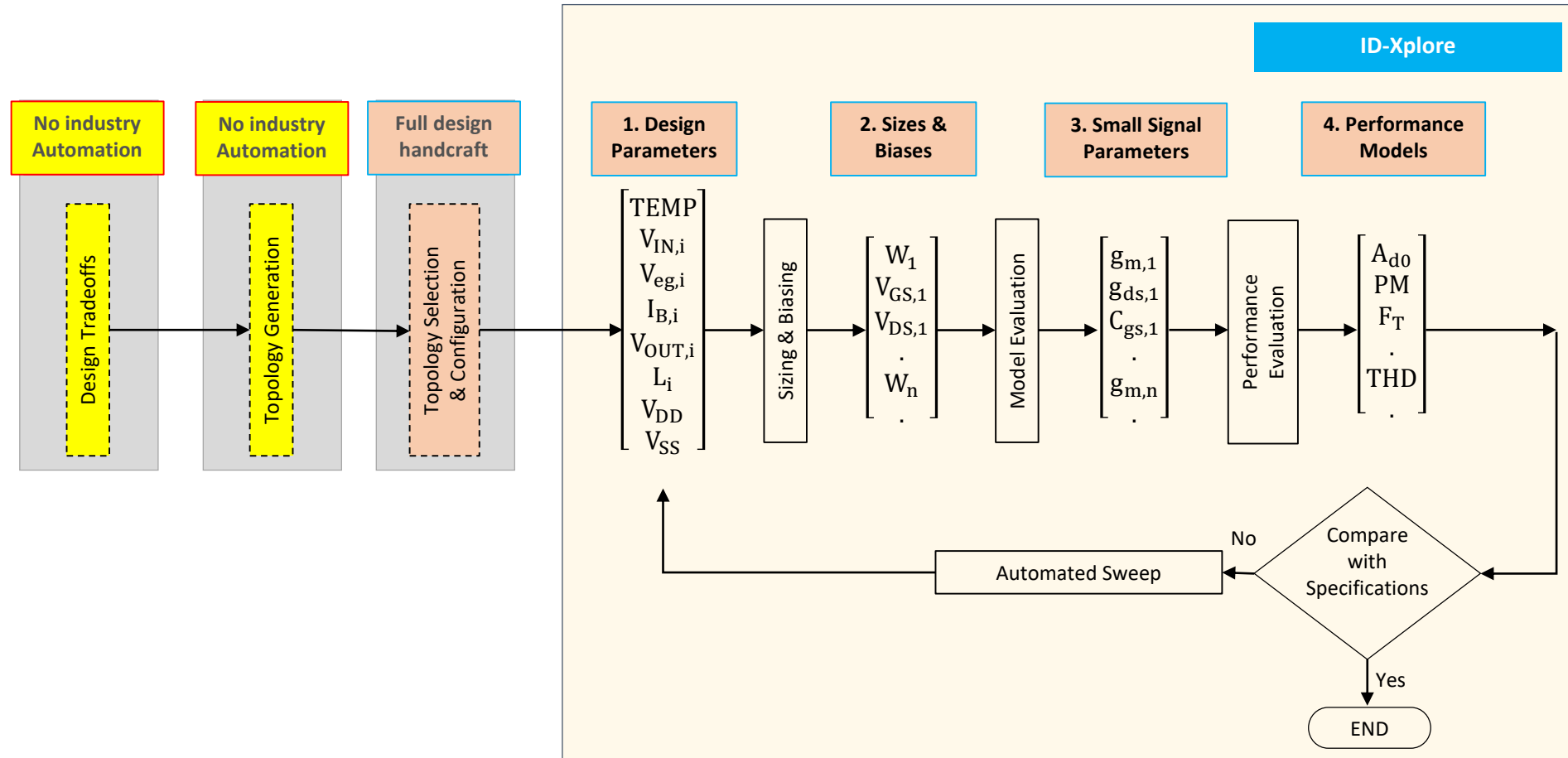
Scheduler

Allocator

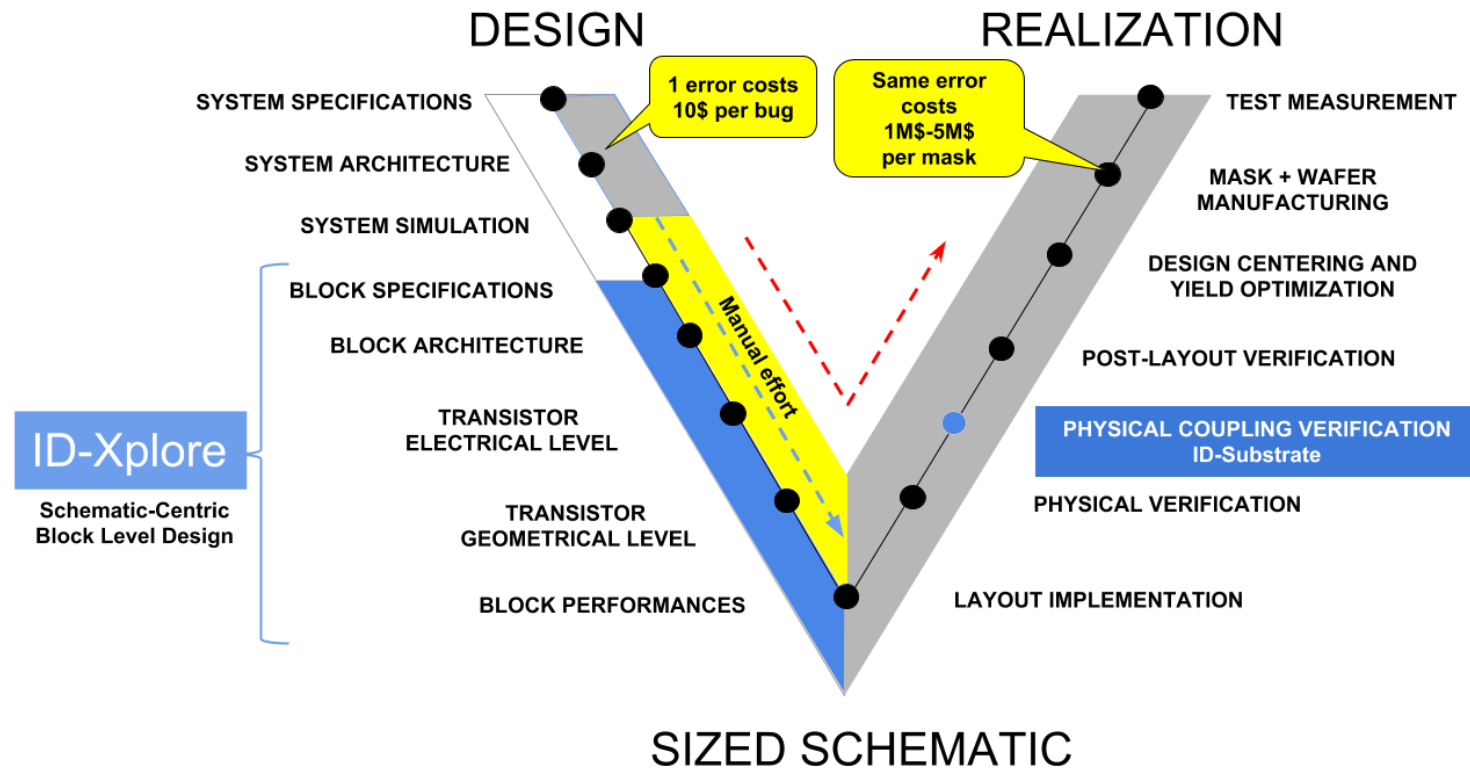
Technology Mapper



Intento Design Product Definition for ID-Xplore™



From Block Specification to Performance



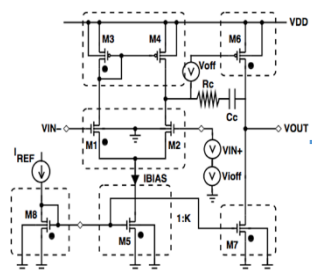
✓ Shorten productivity gap

✓ Shorten quality gap

✓ Avoid design respins

Intento Design Cognitive Front-End Design & Migration Tool

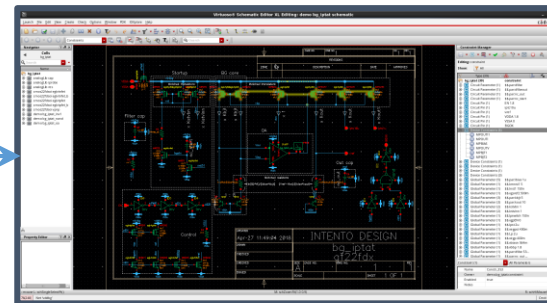
Schematic



Human Tacit Knowledge



Tacit-to-Formal



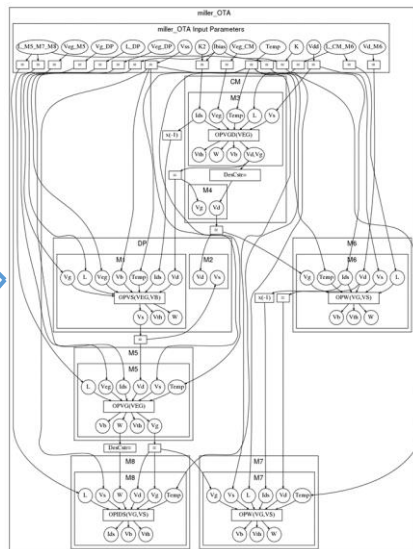
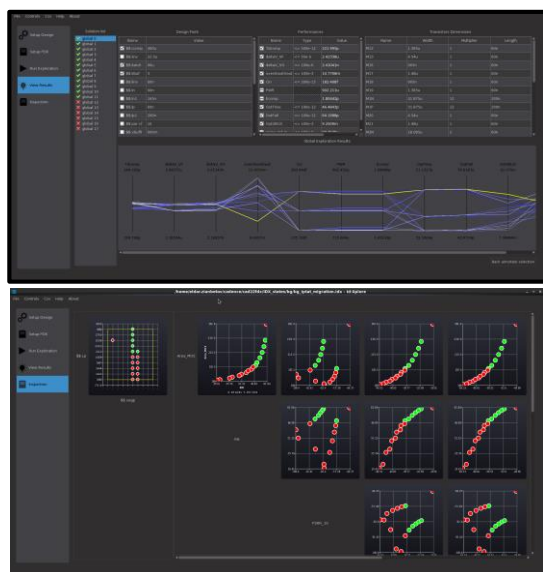
Schematic XL Constraint Manager

Tacit & Formal
Knowledge in
OpenAccess DB

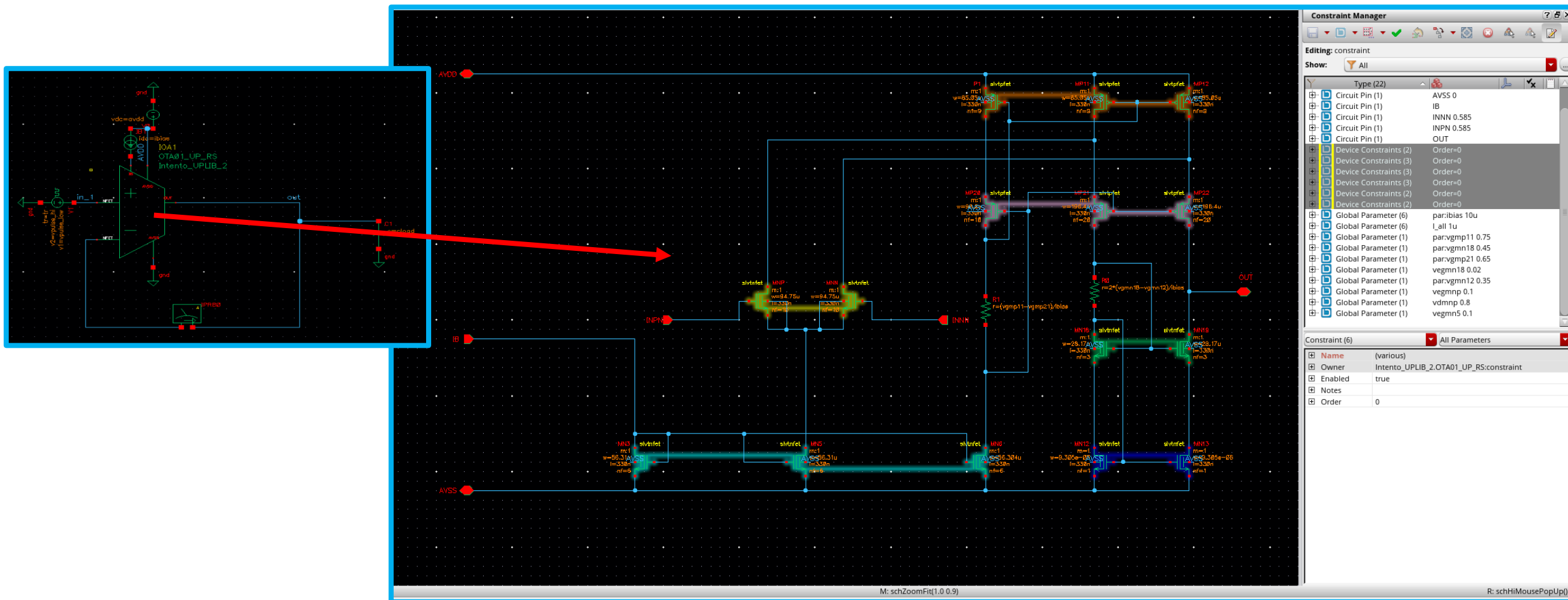


Verification of
Human Reasoning in the
Analog Design

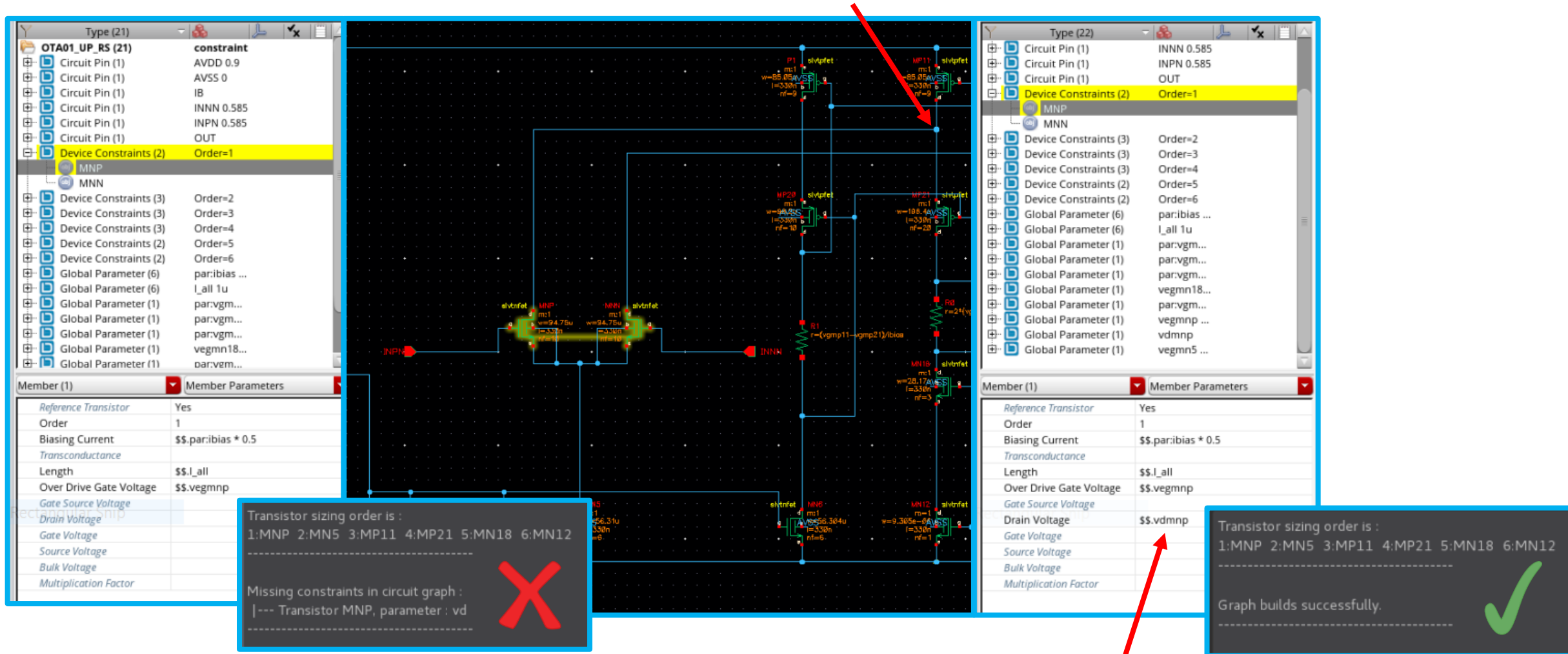
Structured Design Representation



Constraint Manager: Tacit to Formal Knowledge



Verification of Human Reasoning in the Analog Design



Type (21)

Type (21)	constraint
OTA01_UP_RS (21)	
Circuit Pin (1)	AVDD 0.9
Circuit Pin (1)	AVSS 0
Circuit Pin (1)	IB
Circuit Pin (1)	INNN 0.585
Circuit Pin (1)	INPN 0.585
Circuit Pin (1)	OUT
Device Constraints (2)	Order=1
MNP	
MNN	
Device Constraints (3)	Order=2
Device Constraints (3)	Order=3
Device Constraints (3)	Order=4
Device Constraints (2)	Order=5
Device Constraints (2)	Order=6
Global Parameter (6)	par:ibias ...
Global Parameter (6)	I_all 1u
Global Parameter (1)	par:vgm...
Global Parameter (1)	par:vgm...
Global Parameter (1)	par:vgm...
Global Parameter (1)	vegm18...
Global Parameter (1)	vegmnp ...
Global Parameter (1)	par:vegm...

Member (1) Member Parameters

Reference Transistor	Yes
Order	1
Biasing Current	\$\$par:ibias * 0.5
Transconductance	
Length	\$\$I_all
Over Drive Gate Voltage	\$\$vegmnp
Gate Source Voltage	
Drain Voltage	
Gate Voltage	
Source Voltage	
Bulk Voltage	
Multiplication Factor	

Transistor sizing order is :
1:MNP 2:MN5 3:MP11 4:MP21 5:MN18 6:MN12

Missing constraints in circuit graph :
|--- Transistor MNP, parameter : vd

Type (22)

Type (22)	
Circuit Pin (1)	INNN 0.585
Circuit Pin (1)	INPN 0.585
Circuit Pin (1)	OUT
Device Constraints (2)	Order=1
MNP	
MNN	
Device Constraints (3)	Order=2
Device Constraints (3)	Order=3
Device Constraints (3)	Order=4
Device Constraints (2)	Order=5
Device Constraints (2)	Order=6
Global Parameter (6)	par:ibias ...
Global Parameter (6)	I_all 1u
Global Parameter (1)	par:vgm...
Global Parameter (1)	par:vgm...
Global Parameter (1)	par:vgm...
Global Parameter (1)	vegm18...
Global Parameter (1)	par:vgm...
Global Parameter (1)	vegmnp ...
Global Parameter (1)	vegm5 ...

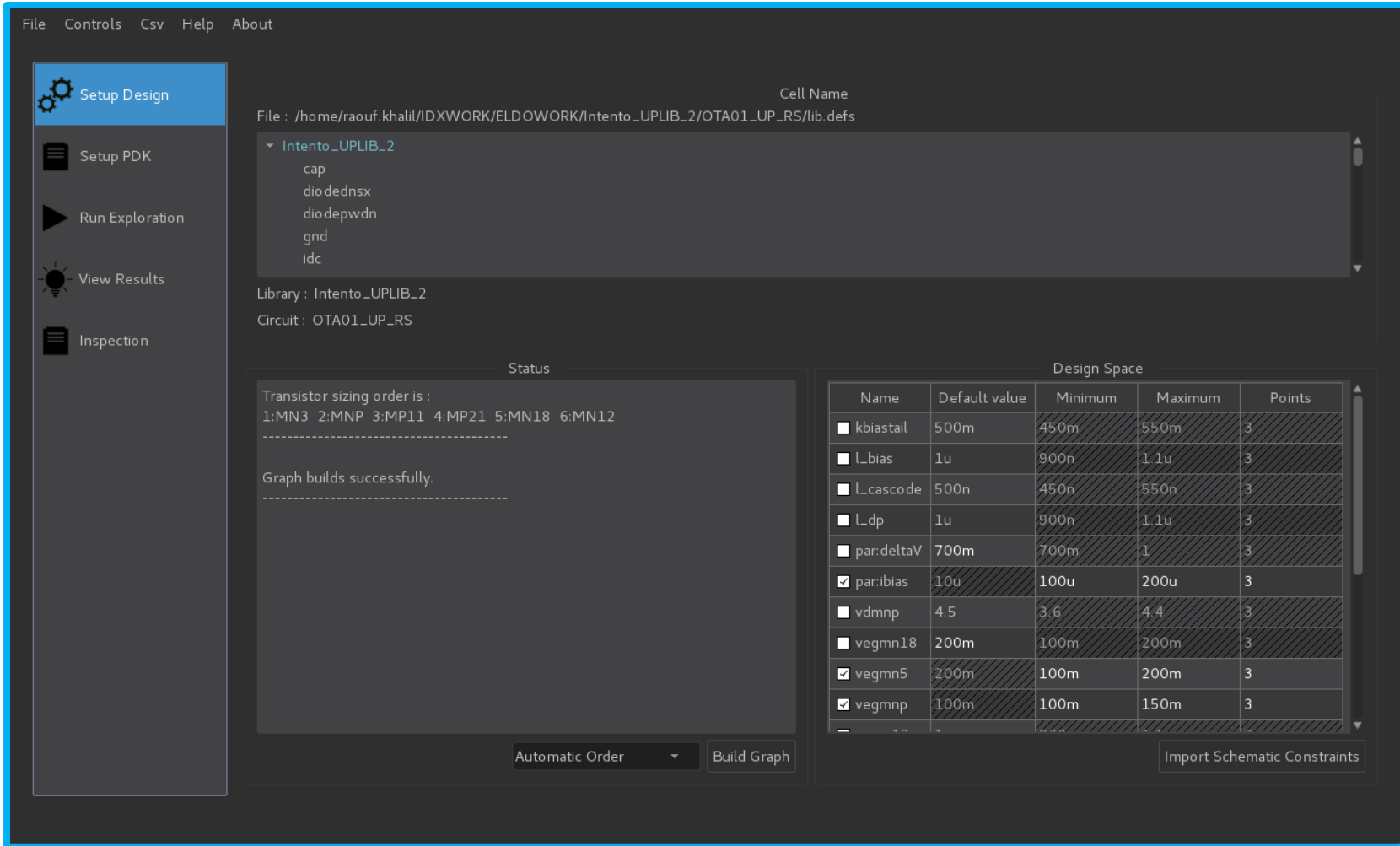
Member (1) Member Parameters

Reference Transistor	Yes
Order	1
Biasing Current	\$\$par:ibias * 0.5
Transconductance	
Length	\$\$I_all
Over Drive Gate Voltage	\$\$vegmnp
Gate Source Voltage	
Drain Voltage	\$\$vdmnp
Gate Voltage	
Source Voltage	
Bulk Voltage	
Multiplication Factor	

Transistor sizing order is :
1:MNP 2:MN5 3:MP11 4:MP21 5:MN18 6:MN12

Graph builds successfully.

Setup Design Space for AMS 0.35 μ m with $V_{DD} = 5V$



The screenshot shows the software interface with the following components:

- Left Sidebar:**
 - Setup Design (selected)
 - Setup PDK
 - Run Exploration
 - View Results
 - Inspection
- Top Menu:** File, Controls, Csv, Help, About
- Cell Name:** /home/raouf.khalil/IDXWORK/ELDOWORK/Intento_UPLIB_2/OTA01_UP_RS/lib.defs
- Library:** Intento_UPLIB_2
- Circuit:** OTA01_UP_RS
- Status:**

Transistor sizing order is :
1:MN3 2:MNP 3:MP11 4:MP21 5:MN18 6:MN12

Graph builds successfully.
- Design Space Table:**

Name	Default value	Minimum	Maximum	Points
<input type="checkbox"/> kbiastail	500m	450m	550m	3
<input type="checkbox"/> l_bias	1u	900n	1.1u	3
<input type="checkbox"/> l_cascode	500n	450n	550n	3
<input type="checkbox"/> l_dp	1u	900n	1.1u	3
<input type="checkbox"/> par:deltaV	700m	700m	1	3
<input checked="" type="checkbox"/> par:ibias	10u	100u	200u	3
<input type="checkbox"/> vdmnp	4.5	3.6	4.4	3
<input type="checkbox"/> vegmn18	200m	100m	200m	3
<input checked="" type="checkbox"/> vegmn5	200m	100m	200m	3
<input checked="" type="checkbox"/> vegmnp	100m	100m	150m	3
- Buttons:** Automatic Order (dropdown), Build Graph, Import Schematic Constraints

Setup Design Space for AMS 0.35 μ m with $V_{DD} = 5V$

File Controls Csv Help About

Setup Design

Setup PDK

Run Exploration

View Results

Inspection

Select Simulator

Spectre /OTA01_UP_RS/IDX_SIZING/sizing_netlist.scs

Select Calculation Type

Multiplier

Nfinger

Setup Technology Constraints

Transistor name	Wmin per finger	Wmax per finger	Lmin	Lmax	Multiplier Max	NFinger Max	
IDX_SIZING_Min_n...	1u	20u	1u	5u			w
IDX_SIZING_Mp_p...	1u	20u	1u	5u			w

Import Remove

Testbench Specifications

Name	Type
<input checked="" type="checkbox"/> PhaseMargFreq_std	
<input checked="" type="checkbox"/> GainMargin_std	
<input checked="" type="checkbox"/> PhaseMargin_std	
<input checked="" type="checkbox"/> GainMargFreq_stddev	
<input checked="" type="checkbox"/> CurrentComp_std	
<input checked="" type="checkbox"/> offset_std	
<input checked="" type="checkbox"/> /home/raouf.khalil/IDWORK/ELDOWORK/Intento_UPLIB_2/OTA01_UP_RS/IDX_ADEXL_TESTS/Intento_UPLIB_2/tb_OTA01_IDT/adexl_all/test_load1p/...	
<input checked="" type="checkbox"/> Loop_Gain_Phase	
<input checked="" type="checkbox"/> Loop_Gain_dB20	

Import Remove

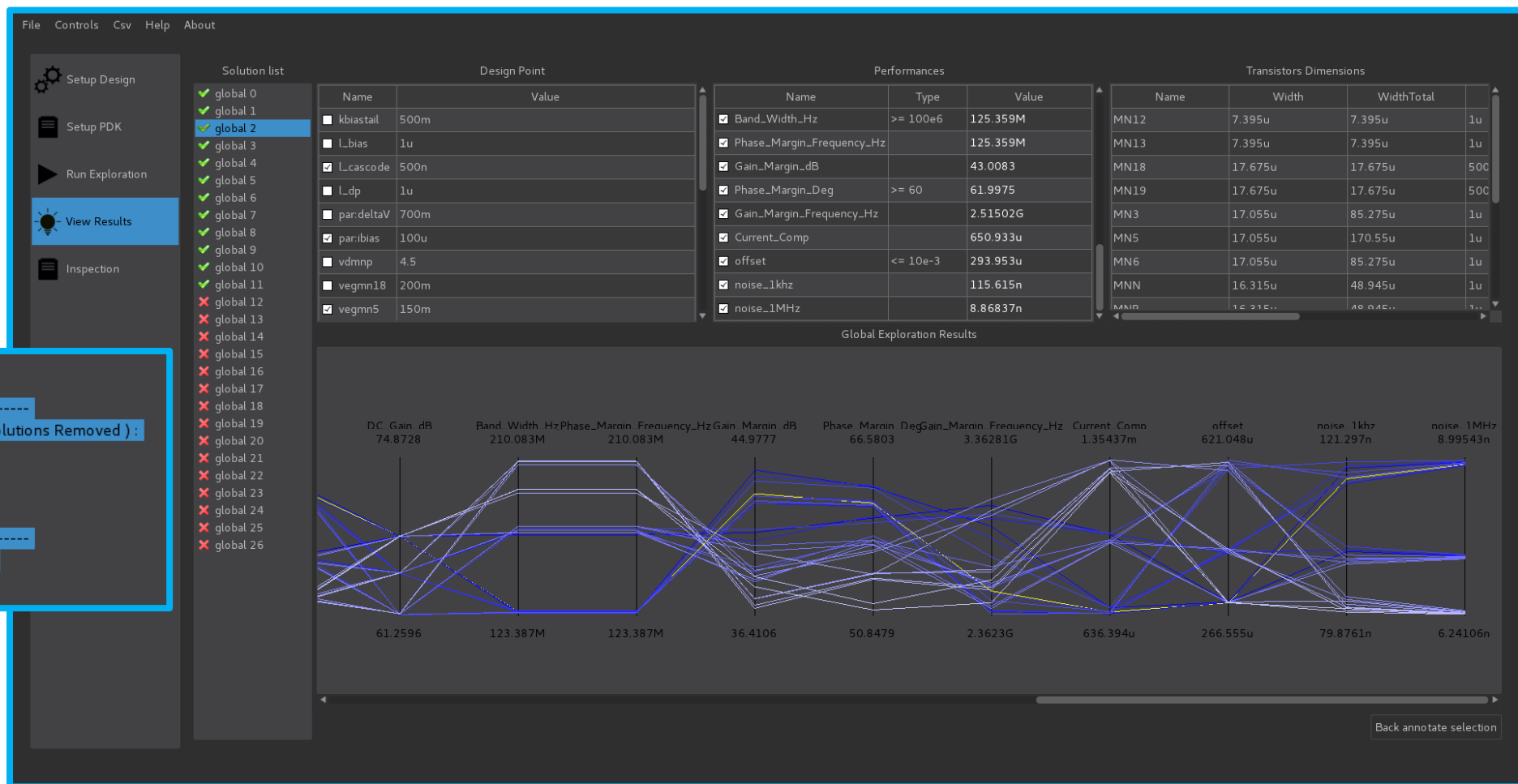
adexl_all

Results

Name	Type	Details	EvalType	Plot	Save	Spec
Loop Gain Phase	expr	phaseDegUnwrapped(getData("...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
Loop Gain dB20	expr	db(mag(getData("loopGain" ?re...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
DC Gain dB	expr	value(db(mag(getData("loopGai...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 60
Band Width Hz	expr	getData("phaseMarginFreq" ?re...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 100M
Phase Margin Frequency Hz	expr	getData("phaseMarginFreq" ?re...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
Gain Margin dB	expr	getData("gainMargin" ?result "st...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
Phase Margin Deg	expr	getData("phaseMargin" ?result "...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	> 60
Gain Margin Frequency Hz	expr	getData("gainMarginFreq" ?resu...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
Current Comp	expr	abs(pv("V0" *i" ?result "dcOpInf...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
offset	expr	abs((v("/out" ?result "dcOp") - v(...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	< 10m
noise_1khz	expr	value(getData("/in" ?result "nois...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
noise_1MHz	expr	value(getData("/in" ?result "nois...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
DCgain_mean	expr	average(value(db(mag(getData("...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
BandWidth_mean	expr	average(getData("phaseMarginF...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
PhaseMargFreq_mean	expr	average(getData("phaseMarginF...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
GainMargin_mean	expr	average(getData("gainMargin" ?...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
PhaseMargin_mean	expr	average(getData("phaseMargin"...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
GainMargFreq_mean	expr	average(getData("gainMarginFr...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
CurrentComp_mean	expr	average(abs(pv("V0" *i" ?result "...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
offset_mean	expr	average(abs((v("/out" ?result "dc...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
DCgain_std	expr	stddev(value(db(mag(getData("l...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
BandWidth_std	expr	stddev(getData("phaseMarginFr...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
PhaseMargFreq_std	expr	stddev(getData("phaseMarginFr...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
GainMargin_std	expr	stddev(getData("gainMargin" ?r...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
PhaseMargin_std	expr	stddev(getData("phaseMargin" ...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
GainMargFreq_stddev	expr	stddev(getData("gainMarginFre...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
CurrentComp_std	expr	stddev(abs(pv("V0" *i" ?result "d...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
offset_std	expr	stddev(abs((v("/out" ?result "dc...	point	<input checked="" type="checkbox"/>	<input type="checkbox"/>	

Monte-Carlo Analysis

View Design Tradeoffs for AMS 0.35 μ m with $V_{DD} = 5V$



TOTAL DURATION : 18 min 53 s

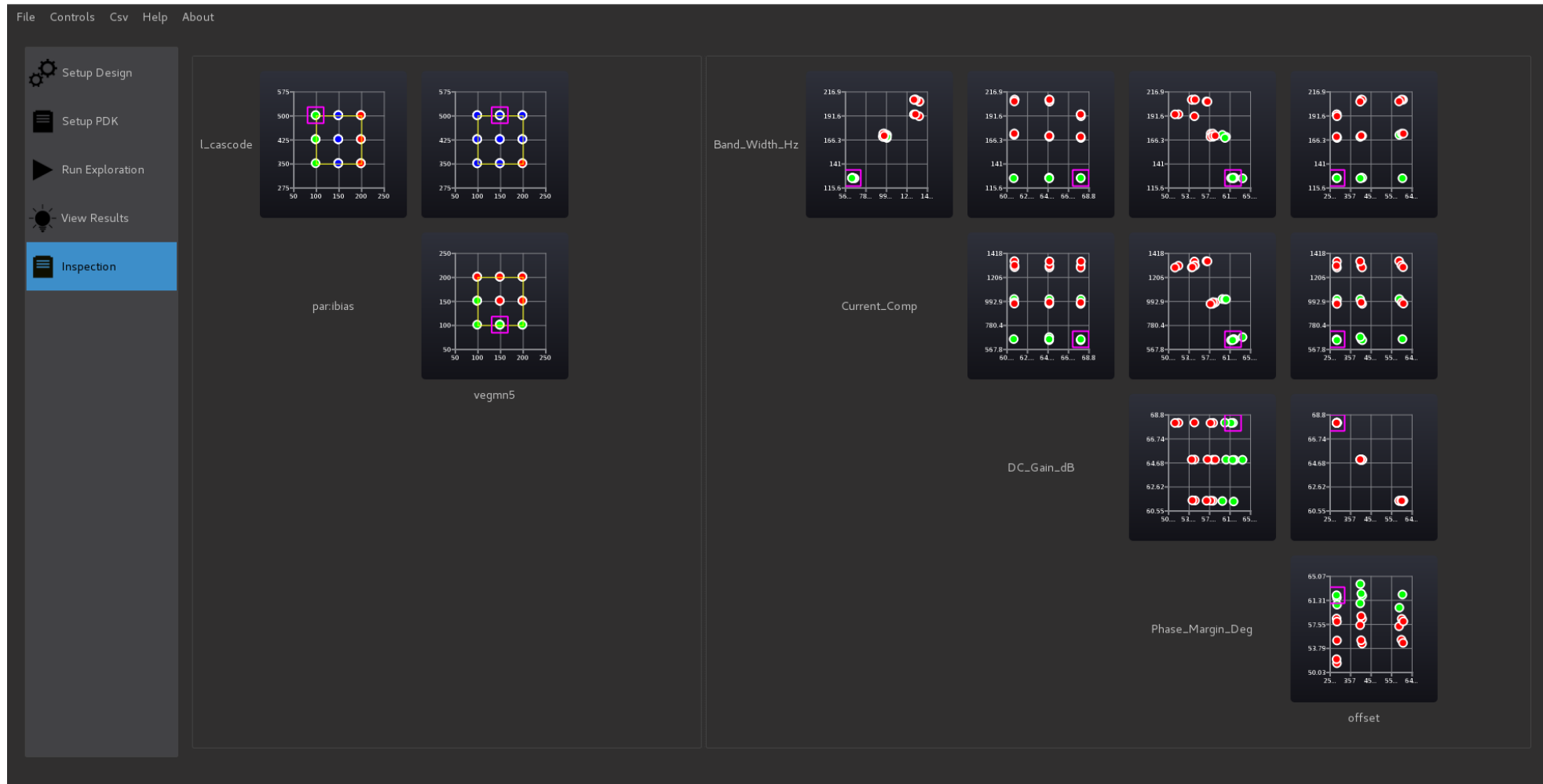
SUMMARY OF THE EVALUATED SOLUTIONS (0 Duplicate Solutions Removed) :

- 12 VALID - all specifications are met
- 15 SOFT VALID - some specifications are met
- 0 INVALID - no specifications are met
- 0 NOT EVALUATED - see log for details

The Number Of Calls In Parallelized Peano Exploration Is : 27

==== END Of Parallelized Peano Exploration ====

Inspect Design Space for AMS 0.35 μm with $V_{DD} = 5V$

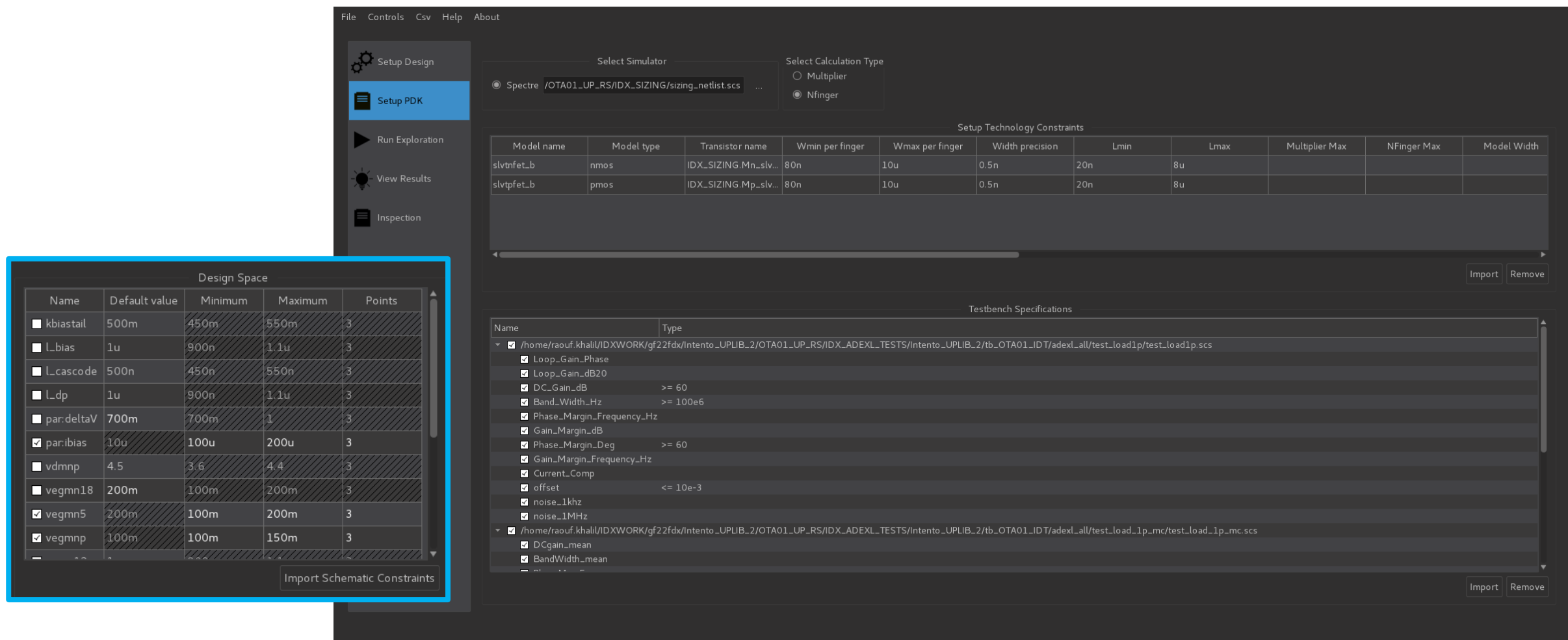


Front-End Signoff Simulation with ADE-Assembler for AMS 0.35 μ m with $V_{DD} = 5V$

Test	Output	Nominal	Spec	Weight	Pass/Fail
test_load_1p_mc	DCgain_mean	67.95			
test_load_1p_mc	BandWidth_mean	124.9M			
test_load_1p_mc	PhaseMargFreq...	124.9M			
test_load_1p_mc	GainMargin_me...	43.09			
test_load_1p_mc	PhaseMargin_m...	62.04			
test_load_1p_mc	GainMargFreq...	2.536G			
test_load_1p_mc	CurrentComp...	651.7u			
test_load_1p_mc	offset_mean	2.314m			
test_load_1p_mc	DCgain_std	1.316			
test_load_1p_mc	BandWidth_std	3.392M			
test_load_1p_mc	PhaseMargFreq...	3.392M			
test_load_1p_mc	GainMargin_std	443.6m			
test_load_1p_mc	PhaseMargin_std	929m			
test_load_1p_mc	GainMargFreq_s...	105M			
test_load_1p_mc	CurrentComp_std	9.851u			
test_load_1p_mc	offset_std	1.68m			
test_load1p	Loop Gain Phase				
test_load1p	Loop Gain dB20				
test_load1p	DC Gain dB	68.06	> 60		pass
test_load1p	Band Width Hz	125.3M	> 100M		pass
test_load1p	Phase Margin Fr...	125.3M			
test_load1p	Gain Margin dB	43.2			
test_load1p	Phase Margin Deg	62.13	> 60		pass
test_load1p	Gain Margin Fre...	2.565G			
test_load1p	Current Comp	653.3u			
test_load1p	offset	293.7u	< 10m		pass
test_load1p	noise_1khz	116n			
test_load1p	noise_1MHz	8.874n			

Performances		
Name	Type	Value
<input checked="" type="checkbox"/> DCgain_mean		67.9459
<input checked="" type="checkbox"/> BandWidth_mean		124.935M
<input checked="" type="checkbox"/> PhaseMargFreq_mean		124.935M
<input checked="" type="checkbox"/> GainMargin_mean		43.0852
<input checked="" type="checkbox"/> PhaseMargin_mean		62.0364
<input checked="" type="checkbox"/> GainMargFreq_mean		2.53605G
<input checked="" type="checkbox"/> CurrentComp_mean		651.686u
<input checked="" type="checkbox"/> offset_mean		2.31437m
<input checked="" type="checkbox"/> DCgain_std		1.31612
<input checked="" type="checkbox"/> BandWidth_std		3.3924M
<input checked="" type="checkbox"/> PhaseMargFreq_std		3.3924M
<input checked="" type="checkbox"/> GainMargin_std		443.592m
<input checked="" type="checkbox"/> PhaseMargin_std		929.035m
<input checked="" type="checkbox"/> GainMargFreq_stddev		105.042M
<input checked="" type="checkbox"/> CurrentComp_std		9.85083u
<input checked="" type="checkbox"/> offset_std		1.67999m
<input checked="" type="checkbox"/> DC_Gain_dB	>= 60	68.0559
<input checked="" type="checkbox"/> Band_Width_Hz	>= 100e6	125.332M
<input checked="" type="checkbox"/> Phase_Margin_Frequency_Hz		125.332M
<input checked="" type="checkbox"/> Gain_Margin_dB		43.2011
<input checked="" type="checkbox"/> Phase_Margin_Deg	>= 60	62.1335
<input checked="" type="checkbox"/> Gain_Margin_Frequency_Hz		2.56543G
<input checked="" type="checkbox"/> Current_Comp		653.27u
<input checked="" type="checkbox"/> offset	<= 10e-3	293.733u
<input checked="" type="checkbox"/> noise_1khz		115.977n

Setup Design Space and PDK For Migration to GF 22nm FDX with $V_{DD} = 1.2V$



The screenshot displays the Q56 Design Automation Conference software interface, specifically the 'Setup Design' and 'Setup PDK' sections. The 'Setup Design' section on the left shows a 'Design Space' table with various parameters and their constraints. The 'Setup PDK' section on the right shows the 'Setup Technology Constraints' table and the 'Testbench Specifications' table.

Design Space

Name	Default value	Minimum	Maximum	Points
kbiastail	500m	450m	550m	3
l.bias	1u	900n	1.1u	3
l.cascode	500n	450n	550n	3
l.dp	1u	900n	1.1u	3
par.deltaV	700m	700m	1	3
par.ibias	10u	100u	200u	3
vdmnp	4.5	3.6	4.4	3
vegm18	200m	100m	200m	3
vegm5	200m	100m	200m	3
vegmnp	100m	100m	150m	3

Import Schematic Constraints

Setup PDK

Select Simulator: Spectre /OTA01_UP_RS/IDX_SIZING/sizing_netlist.scs

Select Calculation Type: Multiplier (selected), Nfinger

Setup Technology Constraints

Model name	Model type	Transistor name	Wmin per finger	Wmax per finger	Width precision	Lmin	Lmax	Multiplier Max	NFinger Max	Model Width
slvtnfet_b	nmos	IDX_SIZING.Mn_slv...	80n	10u	0.5n	20n	8u			
slvtpfet_b	pmos	IDX_SIZING.Mp_slv...	80n	10u	0.5n	20n	8u			

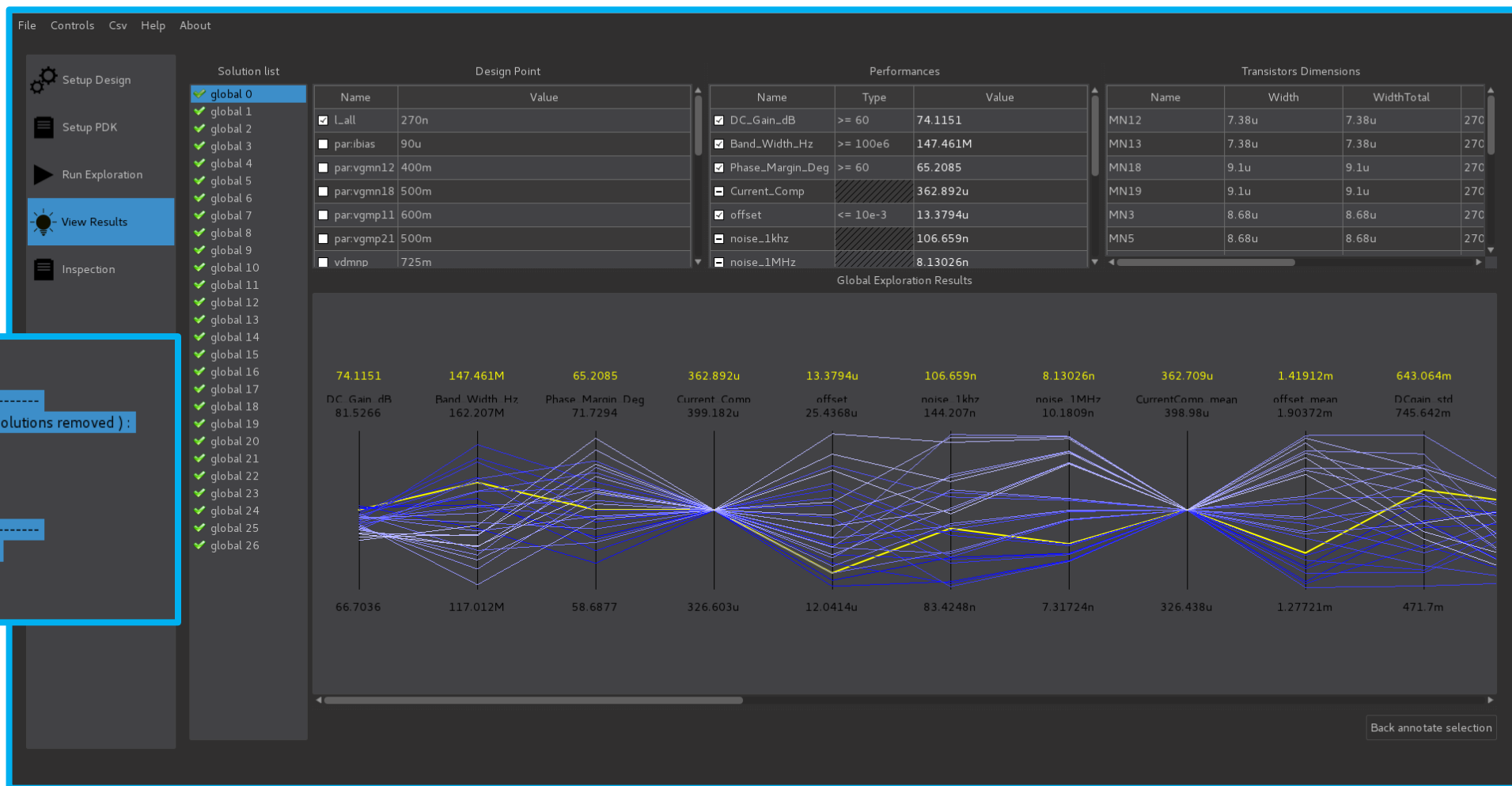
Import Remove

Testbench Specifications

Name	Type
/home/raouf.khalil/IDWORK/gf22fdx/Intento_UPLIB_2/OTA01_UP_RS/IDX_ADEXL_TESTS/Intento_UPLIB_2/tb_OTA01_IDT/adexl_all/test_load1p/test_load1p.scs	
Loop_Gain_Phase	
Loop_Gain_dB20	
DC_Gain_dB	>= 60
Band_Width_Hz	>= 100e6
Phase_Margin_Frequency_Hz	
Gain_Margin_dB	
Phase_Margin_Deg	>= 60
Gain_Margin_Frequency_Hz	
Current_Comp	
offset	<= 10e-3
noise_1khz	
noise_1MHz	
/home/raouf.khalil/IDWORK/gf22fdx/Intento_UPLIB_2/OTA01_UP_RS/IDX_ADEXL_TESTS/Intento_UPLIB_2/tb_OTA01_IDT/adexl_all/test_load_1p_mc/test_load_1p_mc.scs	
DCgain_mean	
BandWidth_mean	

Import Remove

View Design Tradeoffs for GF 22nm FDX with $V_{DD} = 1.2V$



TOTAL DURATION : 404.173 seconds.

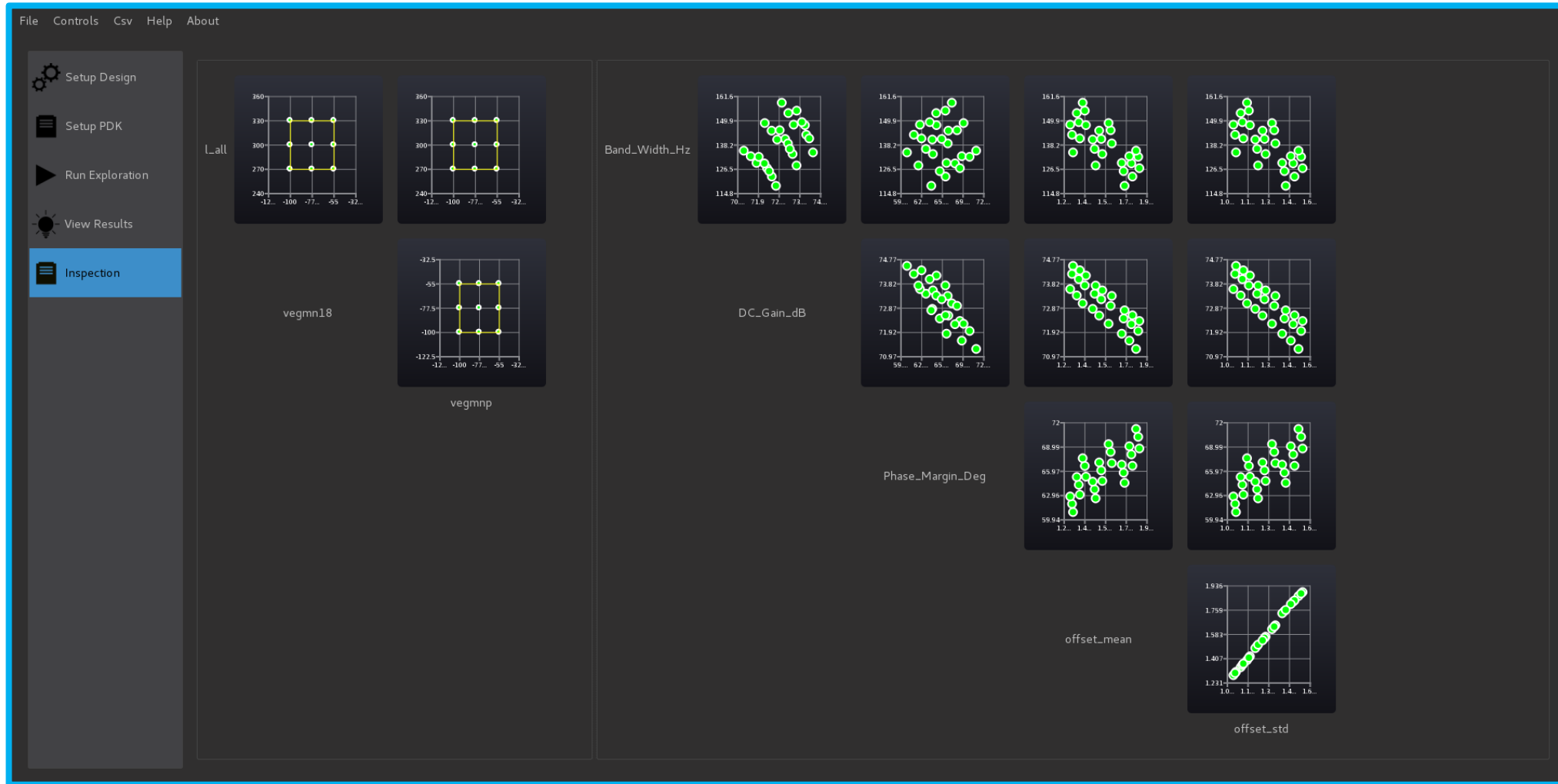
SUMMARY OF THE EVALUATED SOLUTIONS (0 duplicate solutions removed) :

27 VALID
 0 SOFT VALID
 0 INVALID
 0 NOT EVALUATED

The number of calls in parallelized Peano exploration is : 27

==== END of parallelized Peano exploration ====

Inspect Migration Space for GF 22nm FDX with $V_{DD} = 1.2V$



Front-End Signoff Simulation for GF 22nm FDX with $V_{DD} = 1.2V$

Test	Output	Nominal	Spec	Weight	Pass/Fail
test_load1p	Loop Gain Phase				
test_load1p	Loop Gain dB20				
test_load1p	DC Gain dB	69.03	> 60		pass
test_load1p	Band Width Hz	212.6M	> 100M		pass
test_load1p	Phase Margin Fr...	212.6M			
test_load1p	Gain Margin dB	27.73			
test_load1p	Phase Margin Deg	67.35	> 60		pass
test_load1p	Gain Margin Fre...	1.855G			
test_load1p	Current Comp	607.3u			
test_load1p	offset	35.55u	< 10m		pass
test_load1p	noise_1khz	114.8n			
test_load1p	noise_1MHz	8.038n			
test_load_1p_mc	DCgain_mean	69			
test_load_1p_mc	BandWidth_mean	212.8M			
test_load_1p_mc	PhaseMargFreq...	212.8M			
test_load_1p_mc	GainMargin_me...	27.74			
test_load_1p_mc	PhaseMargin_m...	67.35			
test_load_1p_mc	GainMargFreq...	1.86G			
test_load_1p_mc	CurrentComp...	607u			
test_load_1p_mc	offset_mean	1.498m			
test_load_1p_mc	DCgain_std	343.6m			
test_load_1p_mc	BandWidth_std	3.426M			
test_load_1p_mc	PhaseMargFreq...	3.426M			
test_load_1p_mc	GainMargin_std	586.3m			
test_load_1p_mc	PhaseMargin_std	555.8m			
test_load_1p_mc	GainMargFreq_s...	90.27M			
test_load_1p_mc	CurrentComp_std	8.895u			
test_load_1p_mc	offset_std	1.22m			

Performances		
Name	Type	Value
<input checked="" type="checkbox"/> DC_Gain_dB	>= 60	69.0346
<input checked="" type="checkbox"/> Band_Width_Hz	>= 100e6	212.823M
<input checked="" type="checkbox"/> Phase_Margin_Frequency_Hz		212.823M
<input checked="" type="checkbox"/> Gain_Margin_dB		27.4937
<input checked="" type="checkbox"/> Phase_Margin_Deg	>= 60	67.1791
<input checked="" type="checkbox"/> Gain_Margin_Frequency_Hz		1.82981G
<input checked="" type="checkbox"/> Current_Comp		607.258u
<input checked="" type="checkbox"/> offset	<= 10e-3	35.5514u
<input checked="" type="checkbox"/> noise_1khz		114.838n
<input checked="" type="checkbox"/> noise_1MHz		8.03795n
<input checked="" type="checkbox"/> DCgain_mean		69.0025
<input checked="" type="checkbox"/> BandWidth_mean		213.09M
<input checked="" type="checkbox"/> PhaseMargFreq_mean		213.09M
<input checked="" type="checkbox"/> GainMargin_mean		27.4984
<input checked="" type="checkbox"/> PhaseMargin_mean		67.1773
<input checked="" type="checkbox"/> GainMargFreq_mean		1.83483G
<input checked="" type="checkbox"/> CurrentComp_mean		606.979u
<input checked="" type="checkbox"/> offset_mean		1.49838m
<input checked="" type="checkbox"/> DCgain_std		343.577m
<input checked="" type="checkbox"/> BandWidth_std		3.43186M
<input checked="" type="checkbox"/> PhaseMargFreq_std		3.43186M
<input checked="" type="checkbox"/> GainMargin_std		585.76m
<input checked="" type="checkbox"/> PhaseMargin_std		560.974m
<input checked="" type="checkbox"/> GainMargFreq_stddev		89.9229M
<input checked="" type="checkbox"/> CurrentComp_std		8.89481u

Summary

- ✓ ID-Xplore™ is the first industrial cognitive software for very fast analog design and migration of analog IP
- ✓ It is used to produce first-time right analog IP
- ✓ Cognitive means mimicing human design reasoning
- ✓ The Digital transformation shall promote « Cognitive EDA » versus « Traditional EDA »
- ✓ Cognitive EDA will drastically boost design productivity, production quality and time-to-market by at least two order of magnitudes.
- ✓ Cognitive EDA will empower human capacity through efficient collaboration with intelligent machines

Thank you for your kind attention.



Ramy ISKANDER, PhD
CEO
INTENTO DESIGN
office : [+33 1 42 36 14 59](tel:+33142361459)
direct : [+33 9 72 63 27 41](tel:+33972632741)
FR-cell : [+33 6 95 25 15 09](tel:+33695251509)
email : ramy.iskander@intento-design.com
mailing : 10 rue de Richelieu, 75001 Paris, FR
website : www.intento-design.com

